* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The power semiconductor device which it has the following, and the flow of discharge of said 2nd conductivity-type carrier by the side of said 1st conductivity-type emitter of said high resistance base region of an ON state is changed partially, and is characterized by making high carrier concentration by the side of said 1st conductivity-type emitter in said high resistance base region. The 1st conductivity-type emitter region The high resistance base region from which impregnation of the 1st conductivity-type carrier from this 1st conductivity-type emitter region is substantially performed through a channel, and an electric conduction modulation is started by the ON state The 2nd conductivity-type emitter region which pours the 2nd conductivity-type carrier into this high resistance base region The 2nd conductivity-type drain field which discharges the 2nd conductivity-type carrier in said high resistance base region
[Claim 2] The power semiconductor device characterized by providing the following The 1st conductivity-type emitter region The high resistance base region from which impregnation of the 1st conductivity-type carrier from this 1st conductivity-type emitter region is substantially performed through a channel, and an electric conduction modulation is started by the ON state The 2nd conductivity-type emitter region which pours the 2nd conductivity-type carrier into this high resistance base region The part to which it has the 2nd conductivity-type drain field which discharges the 2nd conductivity-type carrier in said high resistance base region, and the carrier concentration in said high resistance base region in an ON state turns into high concentration from the concentration in the core of this high resistance base region by said 1st conductivity-type emitter region side
[Claim 3] The power semiconductor device which is equipped with the following and characterized by the parameter X defined by the formula $X=\{(C-W)+D\}/W$ Becoming satisfying $X>=5$ when distance from the interface of 2W, said 2nd conductivity-type drain layer, and said high resistance base layer to said insulated-gate tip is set to D for the width of face of the field into which the distance between said 2nd conductivity-type drain layers was inserted in 2C and said insulated gate. High resistance base layer The insulated gate embedded with predetermined spacing on this high resistance base layer front face The 1st conductivity-type emitter layer formed in the field across which it faced in this insulated gate The channel field which induction is carried out in said insulated gate, and injects the 1st conductivity-type carrier into said high resistance base layer from said 1st conductivity-type emitter layer, the 2nd conductivity-type emitter layer which injects the 2nd conductivity-type carrier into said high resistance base layer, and the 2nd conductivity-type drain layer which is formed in the field across which said insulated gate faced, and discharges the 2nd conductivity-type carrier from said high resistance base layer
[Claim 4] The power semiconductor device characterized by providing the following The 2nd conductivity-type emitter layer The 1st conductivity-type base layer formed in contact with said 2nd conductivity-type emitter layer The 2nd conductivity-type base layer formed in contact with said 1st conductivity-type base layer The gate electrode by which pad formation was carried out through gate dielectric film in two or more slots formed in the depth which reaches in said 2nd conductivity-type base

layer at said 1st conductivity-type base layer, The channel layer for turn-ofves of the 1st conductivity type formed in contact with the side face of said slot in said 2nd conductivity-type base layer, The 2nd conductivity-type drain layer formed in said channel layer front face for turn-ofves in contact with the side face of said slot, The 1st conductivity-type source layer by which diffusion formation was carried out at the depth which does not exceed said channel layer for turn-ofves in the surface section of said 2nd conductivity-type base layer, The 1st main electrode which contacted coincidence and was formed in said 2nd conductivity-type drain layer and the 1st conductivity-type source layer, and the 2nd main electrode formed in said 2nd conductivity-type emitter layer

[Claim 5] Said slot is a power semiconductor device according to claim 4 characterized by accomplishing the shape of a stripe periodically, being formed, forming said 1st conductivity-type turn-off channel layer and the 2nd conductivity-type drain layer in the slot in every other one, and forming said 1st conductivity-type source layer in the remaining slots.

[Claim 6] It is the power semiconductor device according to claim 4 characterized by for said slot making the shape of a periodic stripe, forming it, forming said 1st conductivity-type turn-off channel layer and the 1st conductivity-type source layer of each other between each slot continuously, and forming said 2nd conductivity-type drain layer in contact with the side face of each slot.

[Claim 7] Said slot is a power semiconductor device according to claim 4 characterized by making the shape of a stripe periodically, being formed and arranging said 1st conductivity-type turn-off channel layer and the 2nd conductivity-type drain, and the 1st conductivity-type source layer by turns along with a longitudinal direction between each slot.

[Claim 8] The power semiconductor device according to claim 4 characterized by forming said 2nd conductivity-type base layer more deeply than said slot.

[Claim 9] The power semiconductor device characterized by providing the following The 2nd conductivity-type emitter layer The 1st conductivity-type base layer formed in contact with said 2nd conductivity-type emitter layer The gate electrode by which pad formation was carried out through gate dielectric film in two or more slots formed in said 1st conductivity-type base layer The channel layer for turn-ofves of the 1st conductivity type formed in said 1st conductivity-type base layer surface section in contact with the side face of said slot, The 2nd conductivity-type drain layer formed in said channel layer front face for turn-ofves in contact with the side face of said slot, The 1st conductivity-type source layer by which diffusion formation was carried out at the depth which does not exceed said channel layer for turn-ofves in the surface section of said 1st conductivity-type base layer, The 1st main electrode which contacted coincidence and was formed in said 2nd conductivity-type drain layer and the 1st conductivity-type source layer, and the 2nd main electrode formed in said 2nd conductivity-type emitter layer

[Claim 10] The power semiconductor device characterized by providing the following. The 1st conductivity-type emitter region The 2nd conductivity-type base layer formed in contact with this 1st conductivity-type emitter region The 1st conductivity-type base layer alternatively formed in contact with said 2nd conductivity-type base layer The gate electrode which was formed in this 1st conductivity-type base layer and by which pad formation was carried out at least through gate dielectric film in the slot on the pair, The 2nd conductivity-type source layer and the 1st conductivity-type drain layer which were formed in said 1st conductivity-type base layer front face between the slots of said pair, The MOS channel for turn-ons of the 1st main electrode formed in contact with said 2nd conductivity-type source layer and the 1st conductivity-type drain, the 2nd main electrode formed in contact with said 1st conductivity-type emitter layer, and the 1st conductivity type formed in contact with the side face of said slot in said 1st conductivity-type base layer

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[Translation done.]

is formed in the surface section of n mold turn-off channel layer 8, and n mold source layer 10 and n mold turn-off channel layer 8 are the same diffusion layers in fact.
[0067] The lateral portion of the slot 5 of p mold base layer 4 which the component of this example has under n mold emitter layer 10 serves as a turn-on channel. Moreover, slot 5 lateral portion of n mold turn-off channel layer 8 under p mold drain layer 9 serves as a turn-off channel. Therefore, the gate electrode 7 by which pad formation was carried out serves both as the object for turn-ons, and the object for turn-ofves into the slot 5 like the previous example.
[0068] The component of this example impresses a forward electrical potential difference to the pad gate electrode 7, and it carries out a turn-on by forming an n-type channel in the slot side face of p mold base layer 4. If a negative electrical potential difference is impressed to the pad gate electrode 7, p mold channel will be formed in the slot lateral portion of n mold turn-off channel layer 8, and a turn-off will be carried out like each previous example.
[0069] Also according to this example, the same effectiveness as each previous example is acquired. Moreover, since the component of this example bears pressure-proofing in the pad gate section like a previous example, it can make low high impurity concentration of p mold base layer 4. For example, it is 1x1016-/cm3 about the peak high impurity concentration of p mold base layer 4. It can consider as extent, it follows on this, and is 1x1017-/cm3 about the peak high impurity concentration of n mold turn-off channel layer 8. It can consider as extent. Consequently, a threshold required to form p mold channel in the slot side face of n mold turn-off channel layer 8 can be made [about / 5V] small, and can perform OFF control in small gate voltage.
[0070] Fig. 34 is the layout of the pad insulated-gate mold semiconductor device of another example of this invention, and drawing 35 and drawing 36 are A-A' of drawing 34 , and a B-B' sectional view, respectively.
[0071] The component of this example is what omitted p mold base layer 4 of the component of the example of drawing 31 - drawing 33 , and serves as the so-called electrostatic-induction thyristor. If the high impurity concentration of n mold base layer 1 and the width of face (width of face of n mold base layer 1 pinched by the slot 5 shown in the cross section of drawing 35) of a slot 5 are set as a suitable value, the potential of the whole part of n mold base layer 1 pinched by the slot 5 is controllable by the pad gate electrode 7.
[0072] A forward electrical potential difference is impressed to the gate electrode 7, if the potential of n mold base layer 1 pinched by the slot 5 is raised, an electron will be poured in from n mold source layer 10, and the turn-on of the component will be carried out. If a negative electrical potential difference is impressed to the gate electrode 7, p mold channel will be formed in the slot side face of n mold turn-off channel layer 8, the carrier of n mold base layer 1 will come to be discharged by the cathode electrode 13 through p mold drain layer 9, and the turn-off of the component will be carried out.
[0073] Drawing 37 is the layout of the pad insulated-gate mold semiconductor device of still more nearly another example, and drawing 38 and drawing 39 are A-A' of drawing 37 , and a B-B' sectional view, respectively.
[0074] This example deforms slightly the component of the example of drawing 31 - drawing 33 . Mutually-independent [of two or more stripe-like slots 5] is carried out, and these perimeters are surrounded by deep p mold base layer 4'. Distribution, the depth, etc. of n mold turn-off channel layer 8, p mold drain layer 9, and n mold source layer 10 which are formed in p mold base layer 4 between the pad gate sections are the same as that of a previous example.
[0075] Drawing 40 is the layout of the pad insulated-gate mold semiconductor device of still more nearly another example, and drawing 41 and drawing 42 are A-A' of drawing 40 , and a B-B' sectional view, respectively.
[0076] This example deforms the component of the example of drawing 34 - drawing 35 like the example of drawing 37 - drawing 39 .
[0077] Also according to these examples, the same effectiveness as each previous example is acquired.
[0078] Drawing 42 - drawing 44 are the examples which transformed the example of drawing 31 - drawing 33 , and made p mold base layer 4 deeper than the pad gate section.

[0079] Drawing 46 - drawing 48 are the examples which transformed the example of drawing 43 - drawing 45 further, and omitted n mold turn-off channel layer 8.
[0080] Drawing 49 - drawing 51 are the examples which omitted the p type **-layer in the structure of drawing 46 - drawing 48 further.
[0081] Also according to these examples, as mentioned above, the optimum design of the width of face and spacing of the geometry of each part, especially the pad gate section can be carried out, injection efficiency of the emitter region of a wide sense can be enlarged enough, and low on resistance can be realized.
[0082] Drawing 52 - drawing 55 are the example of drawing 11 - drawing 14 , and the example which applied the same structure to IGBT, and are **. n mold source layer 10 is formed in contact with the side face of a slot 5, and the cathode electrode 1 contacts at coincidence this n mold source layer 10 and p mold base layer 4 exposed among these.
[0083] Drawing 56 - drawing 58 are the examples which applied the structure of drawing 37 - drawing 39 to IGBT similarly.
[0084] Drawing 59 is the modification of drawing 53 . To emitter width-of-face 2W, if the width of face 2 (C-W) of the pad gate section is not much wide, the dependability of recessing will fall. In such a case, improvement in the yield is achieved by dividing and forming in plurality the slot [**** / one / whose number / originally]. Neither p mold base nor n mold source is formed in a part for n mold base layer exposed into width of face 2 (C-W).
[0085] Drawing 60 - drawing 62 are the layout and A-A' of the unit-cell section of the example which applied this invention to IGBT of a horizontal type, and a B-B' sectional view. By making into a component field the 2nd silicon substrate 22 side of the wafer which pasted up the 1st silicon substrate 20 and 2nd silicon substrate 22 directly on both sides of the oxide film 21 in between, and was obtained, predetermined thickness is processed and let this be n mold base layer 1. The slot 5 of the depth which reaches the pars-basilaris-ossis-occipitalis oxide film 21 is formed in this n mold base layer 1, and it is the gate electrode 71 here. Pad formation is carried out. Surface gate electrode 72 which p mold base layer 4 and n mold source layer 10 are formed between the pad gates, and follows the pad gate electrode 7 through gate oxide 6 on these It is formed. p mold emitter layer 3 is formed in predetermined processing detached building ****** from the pad gate section. Between p mold emitter layer 3 and the pad gate section, it is p. - The mold RISAFU layer 23 is formed.
[0086] Drawing 63 - drawing 65 are the layout and A-A' of the example of IGBT of the horizontal type which transformed the upper example and established the pad gate in the anode side, and a B-B' sectional view. It is p about the 2nd substrate 22 by the side of component formation. - It considers as the mold base layer 24, a slot 5 is formed like the upper example, and it is the pad gate electrode 71 to this. It is formed. n mold base layer 1' is formed between slots, p mold drain layer 3' is formed into it, and it is the surface gate electrode 72 like the upper example on these. It is formed. And predetermined distance ****** n mold source layer 10' is formed from a drain field.
[0087] Drawing 66 - drawing 68 are the example of drawing 1 - drawing 5 , the layout and A-A' of the example which realized the same component as a horizontal-type component, and a B-B' sectional view. The same sign as a previous example is given to a previous example and a corresponding part, and detailed explanation is omitted.
[0088] Drawing 69 - drawing 71 are the layout and A-A' of the component of the example which made reverse the conductivity type of each part of the upper example, and a B-B' sectional view.
[0089] In the example of drawing 31 , although width-of-face dN+ of n mold source layer and width-of-face dP+ of p mold drain layer are in abbreviation etc. by carrying out and are shown in the condition, dN+>dP+, then an ON property are improved and dN+<dP+, then an OFF property are improved. Therefore, a desired property is acquired by carrying out the optimum design of the relation of such width of face. This is the same also in the component of drawing 34 , drawing 37 , drawing 40 , drawing 43 , drawing 46 , drawing 49 , and drawing 56 .
[0090] In order to increase good control maximum current, it is desirable to form dN+ in less than [carrier diffusion length extent or it], and it is desirable to form this greatly in the range which can

guarantee the minimum good control maximum current to lower ON state voltage.
[0091] As mentioned above, according to this invention, with the combination of deep pad insulated-gate structure, the structure which formed the hole-current path where the width of face inserted into this pad insulated gate is narrow at large spacing, and the cathode emitter structure where injection efficiency was suppressed small, it is the component of an electrical-potential-difference drive mold, and about the same property as a GTO thyristor can be realized, without carrying out a latch rise.
[0092] The example of a horizontal-type component is explained further partly.
[0093] Drawing 72 - drawing 74 are the examples which deformed the component of the example of drawing 66 - drawing 68 . At this example, p mold drain layer 9 is the pad gate 72. Not only the field across which it faced but the pad gate 72 Even a cathode side edge section side attachment wall is made to extend, and it is prepared.
[0094] Drawing 75 - drawing 77 are the examples which transformed the structure of drawing 72 - drawing 74 , and are carrying out diffusion formation of the n mold emitter layer 8 at the depth which does not reach a component pars basilaris ossis occipitalis.
[0095] The example of drawing 78 -80 is p+ to a pars basilaris ossis occipitalis as the 2nd substrate 22. p with the type layer 25 - A mold substrate is used and it is n to the front face. - The mold base layer 1 was formed, and also it is the same as that of the example of drawing 76 - drawing 77 .
[0096] Drawing 81 - drawing 83 are what transformed the example of drawing 78 - drawing 80 , and are the pad gate electrode 71. It compares with width of face and is the surface gate electrode 72. Width of face is chosen greatly and it is the pad gate electrode 71. It is the example which formed in the predetermined distance ****** cathode side the turn-on channel field and turn-off channel field which are controlled by the surface gate electrode 72 from the field across which it faced.
[0097] Below drawing 84 shows 1 / 2 cel cross-section structure of other examples of a vertical mold component.
[0098] Drawing 84 is the example it was made not to establish the pad gate like drawing 59 in the field (for width of face L to show) between the fields (for width of face W to show) in which a long electron injection channel is formed.
[0099] Drawing 85 is the example in which pad insulated-gate structure was formed also to the field in which an electron injection channel is not formed in the component of drawing 84 . The gate electrode 7 does not embed a slot 5 completely, but is continuously formed along two or more slots 5. And the CVD oxide film 31 is formed so that a slot 5 may be filled on the component front face in which the gate electrode 7 was formed and flattening of the front face may be carried out.
[0100] Drawing 86 is the example in which p type layer 32 was formed between the slots in which the electron injection channel of the component of drawing 84 is not formed. By forming this p type layer 32, pressure-proofing between the cathode electrode 11 in the field in which a channel is not formed, and n mold base layer 1 can be made into sufficient thing.
[0101] Drawing 87 forms the low resistance metal gates 33, such as aluminum, Ti, and Mo, in this in piles in the component structure of drawing 86 in the field in which it forms in so that the gate electrode 7 may not be completely buried for a slot 5 with the polycrystalline silicon film, and a channel is not formed. The low resistance metal gate 33 top is covered by the organic compound insulators 34, such as polyimide.
[0102] Drawing 88 is the example which carried out pad formation of the low resistance metal gate 33 at the pars basilaris ossis occipitalis of a slot 5 while it forms a slot 5 in the whole field in which a channel is not formed further and forms the polycrystal silicon-gate electrode 7 along this slot 5.
[0103] In each example explained above, in order to enlarge hole-current bypass resistance, it is also effective in the channel field across which it faced at the pad gate to prepare high-concentration n type layer etc. from the low carrier life time layer by an ion implantation etc. or n mold base layer.
[0104] For example, drawing 89 is the example which formed high-concentration n type layer 35 from n mold base layer 1 in the bottom of p mold base layer 4 in the component of drawing 86 . Moreover, drawing 90 is the example in which the low carrier life time layer 36 was formed to the bottom of p mold base layer 4.

[0105] Drawing 91 is the example which transformed the structure of drawing 87 , and is n+ of floating to the upper part of p type layer 32. The mold emitter layer 36 is formed. There is no p mold drain and it has IGBT structure, when a forward electrical potential difference is impressed to the gate electrode 7, the side attachment wall of a slot 5 is met, and the electron injection section is n+ from n mold source layer 10. A channel is formed between the mold emitter layers 36, and it is n+. The mold emitter layer 36 is connected with the cathode electrode 11.
[0106] Drawing 92 is the example which performed the same deformation as drawing 91 to the component of drawing 86 similarly.
[0107] Drawing 93 is the example which formed p mold base layer 4 and p type layer 32 formed at coincidence between the slots of the outside of an electron injection channel field in the component of the example of drawing 85 . Furthermore, drawing 94 is the example which formed p type layer 32 of drawing 93 independently [p mold base layer 4] more deeply than this, and formed n mold emitter layer 36 of floating in the upper part.
[0108] Drawing 95 is p type layer 32 of drawing 91 , and n+. It is the example which shortened the turn-on channel which forms the mold emitter layer 36 more deeply and is controlled by the pad gate 27.
[0109] Each example mentioned above is based on the concept of "making the electron hole bypass resistance by the trench gate electrode structure arranged peculiar increasing, with improving electron injection effectiveness, and reducing the on resistance of a semiconductor device." According to this invention in the important fact which should be observed here, originally, achievement of the lowered on resistance is the point that it is not necessary to adhere to "an increment in electron hole pie pass resistance." Strengthening of carrier impregnation is because it is based on the principle which includes the thought "an increment in electron hole bypass resistance" of "enlarging the ratio of the diffusion current and the electron current of an electron hole."
[0110] Drawing 96 is the layout of IEGT (injection-Enhanced Gate Bipolar Transistor) concerning the further example of this invention, and drawing 97 , drawing 98 , drawing 99 , and drawing 100 are A-A' of drawing 96 , B-B', C-C', and a D-D' sectional view, respectively. In this transistor structure, the same reference mark is given to the same part as the example of drawing 6 - drawing 9 .
[0111] n mold source layer is n+. It is constituted by the mold semi-conductor layer 10. In the surface section of p mold drain layer 4, these source fields 10 are extended to the trench gate electrode 7 at the right angle, as shown in drawing 96 . The cross section relevant to the trench gate electrode 7 of these source fields 10 is shown in drawing 97 . n+ located between each sets of the trench gate electrode 7 of two ****** The type layer 10 is the surface insulating layer 202. It insulates from the first main-electrode layer 11 electrically.
[0112] Between the trench gate electrodes 7 which adjoin as shown in drawing 98 , it is n+. The type layer 10 is p+ which functions as a p mold drain. The mutual array is carried out with the type layer 9. The sectional view of each trench gate electrode 7 shown in drawing 99 is the same as that of it of drawing 9 . p+ The sectional view in a right-angled direction is shown in the trench gate electrode 7 of the mold drain field 9 at drawing 100 . p mold drain layer 9 located between each sets of the trench gate electrode 7 of two ****** in the same manners as the case of drawing 97 in here is the above-mentioned surface insulating layer 202. It insulates from the first main-electrode layer 11 electrically. The concrete dimension of this transistor structure is the same as that of it in the device of drawing 1 - drawing 5 , and is good.
[0113] The actuation of IEGT in this example is as follows. If the electrical potential difference of straight polarity is impressed to the gate electrode 7 to the cathode electrode 11, the turn-on channel located in the periphery of p mold base layer 4 will flow. An electron is injected into n mold base layer 1 from n mold source layer 10, and causes an electric conduction modulation in n mold base layer 1. Thereby, the turn-on of the IEGT is carried out by IGBT actuation.
[0114] If the electrical potential difference of negative polarity is impressed to the gate electrode 7 to the cathode electrode 11, impregnation of the electron from the above-mentioned turn-on channel field will stop. An inversion layer is formed in the side-face part (slot side lateral portion) which faces the trench 5 of the trench gate section. By well-known p channel MOS transistor actuation, the carrier in p mold base

layer 4 is discharged by the cathode electrode 11 through p mold drain layer 9. The turn-off of the semiconductor device is carried out. In the case of this example, the parasitism thyristor from which this device is constituted also from a turn-on condition by n mold source layer 10, p mold base layer 4, n mold base layer 1, and p mold emitter layer 3 is arranged especially like the above-mentioned explanation so that a latch rise may not be carried out. If an on-channel closes, the electron injection from n mold source layer 10 will stop immediately.

[0115] P+ which according to IEBT is located between the trench gate 7 of a certain pair, and the trench gate electrode of this pair, and is insulated from the electrode 11 The mold drain layer 9 and this insulated P+ Other P+ which is in contact with ****** and an electrode 11 on both sides of a mold drain layer and the corresponding trench gate electrode 7 A "unit cell" is prescribed by the mold drain layer 9.

[0116] p+ in contact with an electrode 11 It is possible to avoid the technical difficulty of forming the trench slot (2C-2W) where width of face is wide, and to raise effectiveness equivalent to the trench slot where width of face is wide between drain layers, by forming the field which was surrounded by the trench slot where width of face is comparatively narrow, and was insulated with the electrode 11.

[0117] On resistance low enough can be obtained not being made to carry out thyristor actuation of (the example was already shown) and the device by arranging appropriately the depth of two or more trench gate electrodes 7, spacing, and a number. The contact to p mold drain layer 9 of the main electrode 11 of IEGT "thinned out" is contributing to implementation of the on resistance to which the bypass current of an electron hole decreased namely, decreased. Moreover, in this example, a parasitism thyristor does not carry out a latch rise by the ON state, but a turn-off channel opens on the occasion of a turn-off, and the bypass way of the flow of an electron hole is formed. Therefore, once a latch rise is carried out, the present GTO thyristor ratio **** and the maximum breaking current capacity which were constituted so that a turn-off might be carried out are strengthened.

[0118] Explanation is added about the point that big electron injection effectiveness is acquired, by arranging the ratio to all the currents of the electron hole diffusion current here.

[0119] When the high impurity concentration of the emitter region (an example is shown in the part surrounded with the broken line in drawing 21) of a wide sense is comparatively low, For example, when there is a part which produces the conduction modulation of n-p in the emitter region of a wide sense etc., By establishing the diffusion current Ip of an electron hole, and structure which enlarges especially the ratio of a lengthwise direction (diffusion current which flows in parallel with the direction of an anode-cathode of a component), and the electron current In (=I-Ip, I: all currents) all over the emitter region of a wide sense The injection efficiency of the emitter region of a wide sense can be increased, and the on resistance of a component can be decreased.

[0120] It considers as the emitter side carrier concentration n (cm-3) of the wide sense of the hole current Jp (A/cm2) and n-base which flow to the emitter region of a wide sense (n in drawing 29).

[0121] If the hole current which flows to the emitter region of a wide sense considers only as the diffusion current of the carrier of a lengthwise direction (the direction of A-K) Jp=2andmup**k**T**W**n/(C-D) -- It can express (12). Here, mup is [the Boltzmann multiplier and T of hole mobility and k] temperature.

[0122] Injection efficiency gammap of the electron hole of the emitter region of a wide sense gammap=Jp/J=Jp/(Jn+Jp)
= 2microp**k**T**W**ns/(C-D-J) If (C-D) and the value of gammap=2 (mup-k-T-n/J) and Ygammap will be made into mup=500, k-T=4.14x10-21, and J=100 A/cm2 gammap=2x(500x4.14x10-21 / 100) x1x1016xY [--(13) Y=W] =4.14x10-4 and Y -- (16) gammap is, when injection efficiency is sufficiently low. gammap=Jp/(Jn+Jp) =mup/(mun+mup) =0.3 -- (17) It is extent. That is, it is that the injection efficiency of the emitter region of a wide sense is large. gammap<0.3 -- Y which is (18) and fulfills this condition 4.14x10-4 and Y< 0.3 Y< 0.3 / 4.14x10-4 Y< 7.25x102 (cm-1) -- (19) -- the case where ON state voltage is comparatively high -- the time of n= 7x1015 Y< 1.0x103 (cm-1) -- it is (20).

[0123] That is, even if the injection efficiency of the impurity diffused layer which is in contact with the cathode electrode by designing Parameter Y in the above-mentioned range is low, the injection efficiency of the emitter region of a wide sense can be increased. That is, it is possible to be able to

make are recording of the carrier in the ON state of a high resistance base layer increase, and to decrease the on resistance of a component.

[0124] Thus, when a component is arranged, the cathode diffusion layer with low injection efficiency can guarantee switching of a high current controllability and a high speed, and can also realize low component on resistance to coincidence by the increment in the injection efficiency of the emitter region of the wide sense which is the effectiveness of this invention.

[0125] When the emitter region of a wide sense is trench structure like drawing 20 , the value of Y is decided by D, C, and W of drawing 20 as mentioned above.

[0126] Moreover, when the high place (Jp flows by resistance) of high impurity concentration and the low place of high impurity concentration live together in the emitter region of a wide sense, the injection efficiency of the emitter region of a wide sense needs to take into consideration both above-mentioned parameters X and Y.

[0127] The cross-section structure of drawing 100 deforms, as shown in drawing 101 . Here, it is n+. The mold source layer 10 is prolonged so that it may join to the both-sides end face of each trench 5 with which the trench gate electrode 7 was embedded.

[0128] IEGT shown in drawing 102 - Fig. 106 is the combination of the device of drawing 96 - drawing 100 , and the device of drawing 6 - drawing 9 fundamentally. In other words, this IEGT is every p+. The mold drain layer 9 is a point with a "ladder mold flat-surface configuration", and differs from drawing 96 - drawing 100 characteristic. n mold source layer 10 especially explained by drawing 7 is p+. It is formed in the surface section of the mold base layer 4. p mold drain layer 9 is arranged so that it may join to both the upper part side edge of each trench 5 into n mold source layer 10. p mold drain layer 9 is shallower than n mold source layer 10. The part of n mold source layer 10 sandwiched by the pars basilaris ossis occipitalis of p mold drain layer 9 and p mold drain layer 4 functions as an n mold turn-off channel layer 10 explained by drawing 7 . The central part of n mold source layer 10 between two adjoining trench gate electrodes 7 is equivalent to n mold source layer 10 of drawing 2 . If a substrate front-face top is seen, between two adjoining trench gate electrodes 7, p mold drain layer 9 will surround n mold source layer 10 superficially, and, thereby, will present the flat-surface configuration of a ladder mold.

[0129] it is shown in drawing 104 -- as -- n mold source layer 10 -- p+ if it attaches and sees in the cross-section structure which was deeper than the mold drain layer 9, therefore was shown here -- n mold source layer 10 -- p+ The mold drain layer 9 is enclosed. The cross-section structure of each trench gate electrode 7 shown in drawing 105 is the same as that of it of drawing 99 . it is shown in drawing 106 -- as -- p+ mold drain layer 9 -- surface insulating layer 202 " -- it thins out and carries out -- having -- " -- the electrode 11 is in contact.

[0130] According to IEGT of this example, the trench junction lateral portion of p mold base layer 4 located directly under n mold turn-off channel layer functions as a turn-on channel. Therefore, the both sides of two or more trench gate electrodes 7 can say that they are making the turn-on drive electrode and the turn-off drive electrode serve a double purpose. That is, p channel MOS FET for turn-ofves and n channel MOS FET for turn-ons are **** Misa **** structures inside a device. If a straight polarity electrical potential difference is impressed to the trench gate electrode 7, an n-type channel will be formed in each trench junction lateral portion of p mold base layer 4, with the turn-on of the device will be carried out. At this time, an electron is injected into n mold base layer 1 through the n-type channel which appears by n mold turn-off channel and inversion layer formation from the n mold each source layer 10.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The layout pattern of the insulated-gate mold semiconductor device of the example of this invention.
[Drawing 2] The A-A' sectional view of drawing 1 .
[Drawing 3] The B-B' sectional view of drawing 1 .
[Drawing 4] The C-C' sectional view of drawing 1 .
[Drawing 5] The D-D' sectional view of drawing 1 .
[Drawing 6] The layout pattern of the insulated-gate mold semiconductor device of other examples.
[Drawing 7] The A-A' sectional view of drawing 6 .
[Drawing 8] The B-B' sectional view of drawing 6 .
[Drawing 9] The C-C' sectional view of drawing 6 .
[Drawing 10] The layout pattern of the insulated-gate mold semiconductor device of other examples.
[Drawing 11] The A-A' sectional view of drawing 10 .
[Drawing 12] The B-B' sectional view of drawing 10 .
[Drawing 13] The C-C' sectional view of drawing 10 .
[Drawing 14] The layout pattern of the insulated-gate mold semiconductor device of other examples.
[Drawing 15] The A-A' sectional view of drawing 14 .
[Drawing 16] The B-B' sectional view of drawing 14 .
[Drawing 17] The C-C' sectional view of drawing 14 .
[Drawing 18] The sectional view showing the unit-cell structure of the insulated-gate mold semiconductor device of other examples.
[Drawing 19] A-A' of the component of drawing 18 , and B-B' -- drawing showing the impurity atom concentration profile of 1.
[Drawing 20] The sectional view of the pad insulated-gate mold IBGT of a simulation model.
[Drawing 21] Drawing for explaining the principle of operation of the model of drawing 20 .
[Drawing 22] Drawing showing the depth of the pad gate section of this model, and the relation of current density.
[Drawing 23] Drawing showing the width of face of the pad gate section of this model, and the relation of current density.
[Drawing 24] Drawing showing the width of face of the pad gate section in other conditions of this model, and the relation of current density.
[Drawing 25] Drawing showing the current-voltage characteristic of this model.
[Drawing 26] Drawing showing the current-voltage characteristic in other conditions of this model.
[Drawing 27] Drawing showing the current of this model, and an electrical-potential-difference change property.
[Drawing 28] Drawing showing the relation of the current density of Parameter X (D, W, C) and carrier life time taup, and a component.
[Drawing 29] Drawing showing the carrier concentration distribution by the ON state of a component.

[Drawing 30] Drawing showing the structure which applied this model to the component of the example of drawing 6 .
[Drawing 31] The layout pattern of the insulated-gate mold semiconductor device of other examples.
[Drawing 32] The A-A' sectional view of drawing 31 .
[Drawing 33] The B-B' sectional view of drawing 31 .
[Drawing 34] The layout pattern of the insulated-gate mold semiconductor device of other examples.
[Drawing 35] The A-A' sectional view of drawing 34 .
[Drawing 36] The B-B' sectional view of drawing 34 .
[Drawing 37] The layout pattern of the insulated-gate mold semiconductor device of other examples.
[Drawing 38] The A-A' sectional view of drawing 37 .
[Drawing 39] The B-B' sectional view of drawing 37 .
[Drawing 40] The layout pattern of the insulated-gate mold semiconductor device of other examples.
[Drawing 41] The A-A' sectional view of drawing 40 .
[Drawing 42] The B-B' sectional view of drawing 40 .
[Drawing 43] The layout pattern of the insulated-gate mold semiconductor device of other examples.
[Drawing 44] The A-A' sectional view of drawing 43 .
[Drawing 45] The B-B' sectional view of drawing 43 .
[Drawing 46] The layout pattern of the insulated-gate mold semiconductor device of other examples.
[Drawing 47] The A-A' sectional view of drawing 46 .
[Drawing 48] The B-B' sectional view of drawing 46 .
[Drawing 49] The layout pattern of the insulated-gate mold semiconductor device of other examples.
[Drawing 50] The A-A' sectional view of drawing 49 .
[Drawing 51] The B-B' sectional view of drawing 49 .
[Drawing 52] The layout pattern of the insulated-gate mold semiconductor device of other examples.
[Drawing 53] The A-A' sectional view of drawing 52 .
[Drawing 54] The B-B' sectional view of drawing 52 .
[Drawing 55] The C-C' sectional view of drawing 52 .
[Drawing 56] The layout pattern of the insulated-gate mold semiconductor device of other examples.
[Drawing 57] The A-A' sectional view of drawing 56 .
[Drawing 58] The B-B' sectional view of drawing 56 .
[Drawing 59] Drawing showing the modification of drawing 53 .
[Drawing 60] The layout pattern of the insulated-gate mold semiconductor device of other examples.
[Drawing 61] The A-A' sectional view of drawing 60 .
[Drawing 62] The B-B' sectional view of drawing 60 .
[Drawing 63] The layout pattern of the insulated-gate mold semiconductor device of other examples.
[Drawing 64] The A-A' sectional view of drawing 63 .
[Drawing 65] The B-B' sectional view of drawing 63 .
[Drawing 66] The layout pattern of the insulated-gate mold semiconductor device of other examples.
[Drawing 67] The A-A' sectional view of drawing 66 .
[Drawing 68] The B-B' sectional view of drawing 66 .
[Drawing 69] The layout pattern of the insulated-gate mold semiconductor device of other examples.
[Drawing 70] The A-A' sectional view of drawing 69 .
[Drawing 71] The B-B' sectional view of drawing 69 .
[Drawing 72] The layout pattern of the insulated-gate mold semiconductor device of other examples.
[Drawing 73] The A-A' sectional view of drawing 72 .
[Drawing 74] The B-B' sectional view of drawing 72 .
[Drawing 75] The layout pattern of the insulated-gate mold semiconductor device of other examples.
[Drawing 76] The A-A' sectional view of drawing 75 .
[Drawing 77] The B-B' sectional view of drawing 75 .
[Drawing 78] The layout pattern of the insulated-gate mold semiconductor device of other examples.
[Drawing 79] The A-A' sectional view of drawing 78 .

[Drawing 80] The B-B' sectional view of drawing 78 .
[Drawing 81] The layout pattern of the insulated-gate mold semiconductor device of other examples.
[Drawing 82] The A-A' sectional view of drawing 81 .
[Drawing 83] The B-B' sectional view of drawing 81 .
[Drawing 84] Drawing showing 1 / 2 cel cross-section structure of other examples.
[Drawing 85] Drawing showing 1 / 2 cel cross-section structure of other examples.
[Drawing 86] Drawing showing 1 / 2 cel cross-section structure of other examples.
[Drawing 87] Drawing showing 1 / 2 cel cross-section structure of other examples.
[Drawing 88] Drawing showing 1 / 2 cel cross-section structure of other examples.
[Drawing 89] Drawing showing 1 / 2 cel cross-section structure of other examples.
[Drawing 90] Drawing showing 1 / 2 cel cross-section structure of other examples.
[Drawing 91] Drawing showing 1 / 2 cel cross-section structure of other examples.
[Drawing 92] Drawing showing 1 / 2 cel cross-section structure of other examples.
[Drawing 93] Drawing showing 1 / 2 cel cross-section structure of other examples.
[Drawing 94] Drawing showing 1 / 2 cel cross-section structure of other examples.
[Drawing 95] Drawing showing 1 / 2 cel cross-section structure of other examples.
[Drawing 96] The layout pattern of IEGT of other examples.
[Drawing 97] The A-A' sectional view of drawing 96 .
[Drawing 98] The B-B' sectional view of drawing 96 .
[Drawing 99] The C-C' sectional view of drawing 96 .
[Drawing 100] The D-D' sectional view of drawing 96 .
[Drawing 101] The sectional view showing the modification of drawing 100 .
[Drawing 102] The layout pattern of IEGT of other examples.
[Drawing 103] The A-A' sectional view of drawing 102 .
[Drawing 104] The B-B' sectional view of drawing 102 .
[Drawing 105] The C-C' sectional view of drawing 102 .
[Drawing 106] The D-D' sectional view of drawing 102 .
[Drawing 107] Drawing showing the modification of the horizontal type IGBT of drawing 60 - drawing 83 .
[Drawing 108] Drawing showing the modification of the horizontal type IGBT of drawing 60 - drawing 83 .
[Drawing 109] Drawing showing the modification of the horizontal type IGBT of drawing 60 - drawing 83 .
[Drawing 110] Drawing showing the modification of the horizontal type IGBT of drawing 60 - drawing 83 .
[Drawing 111] Drawing showing the modification of the horizontal type IGBT of drawing 60 - drawing 83 .
[Drawing 112] Drawing showing the modification of the horizontal type IGBT of drawing 60 - drawing 83 .
[Description of Notations]
1 -- n mold base layer,
2 -- n mold buffer layer,
3 -- p mold emitter layer,
4 -- p mold base layer,
5 -- Slot,
6 -- Gate oxide
7 -- Gate electrode,
8 -- n mold turn-off channel layer,
9 -- p mold drain layer,
10 -- n mold source layer,
11 -- Cathode electrode,

12 -- Anode electrode.

[Translation done.]

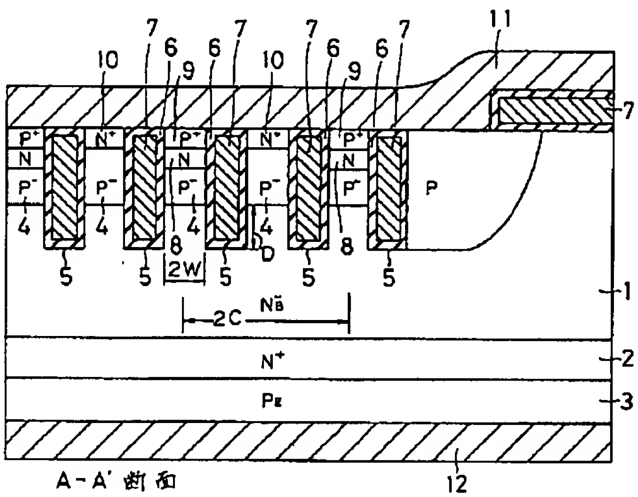
* NOTICES *

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 2]



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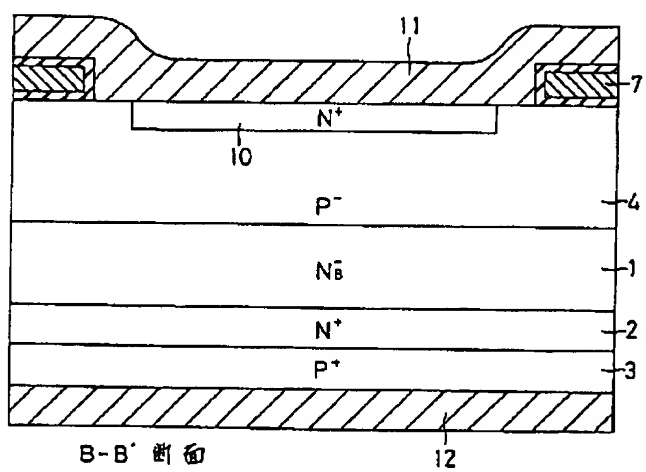

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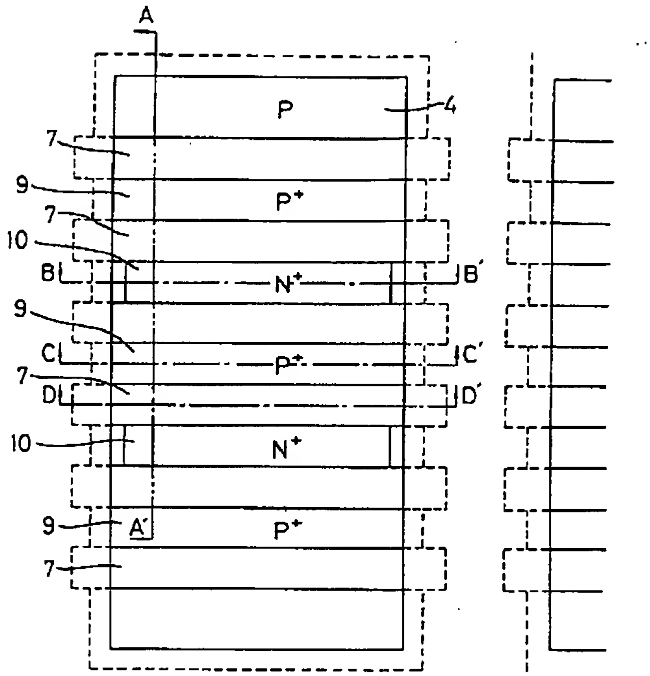

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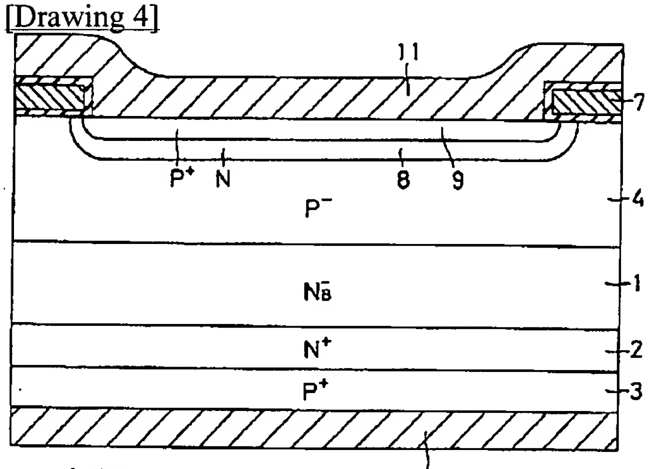
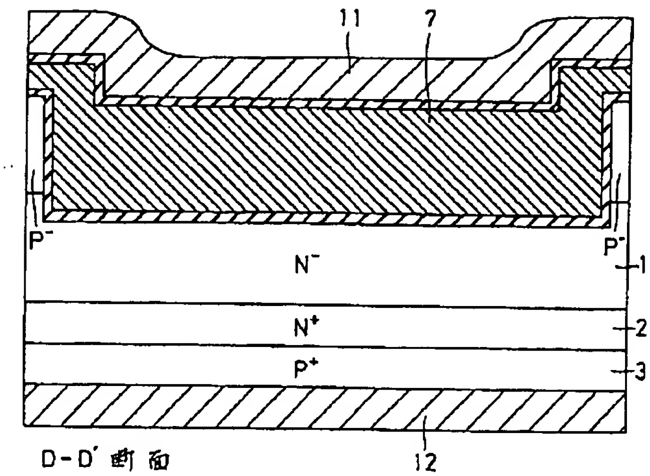


C-C' 断面

[Drawing 5]



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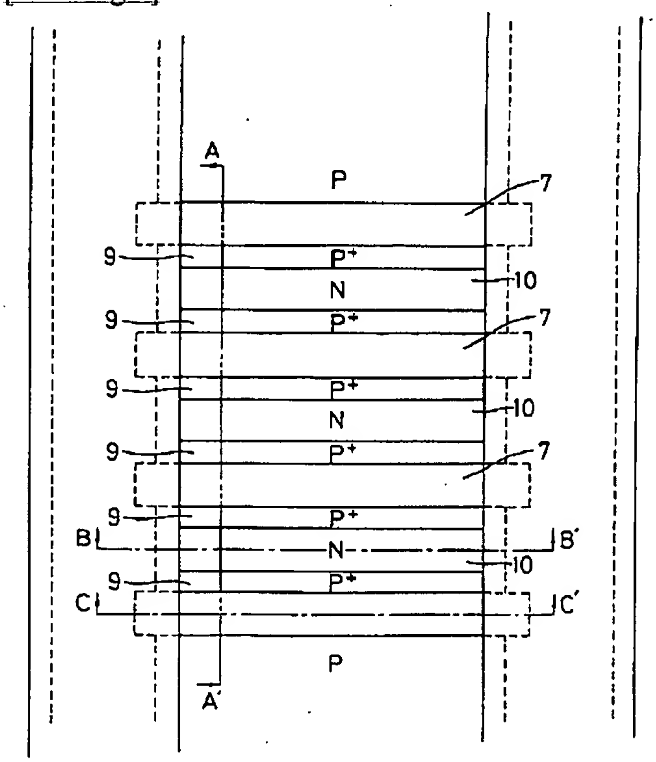

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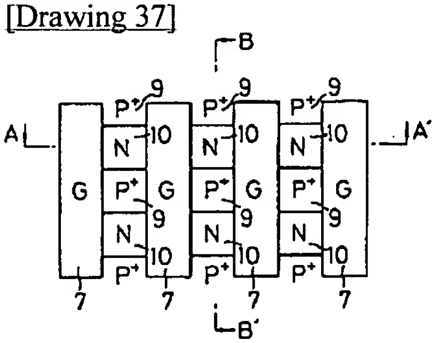

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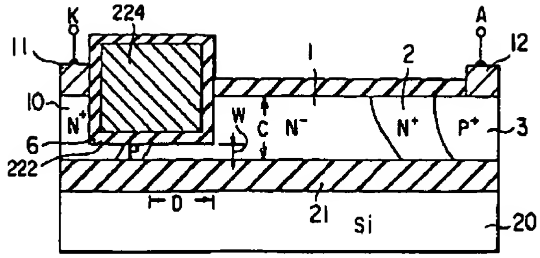

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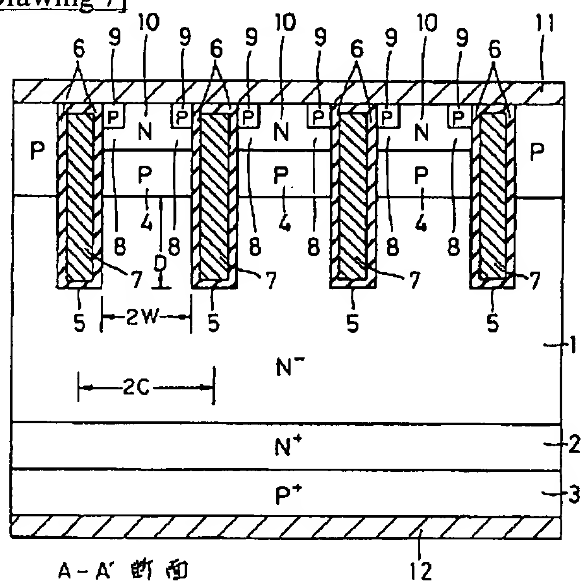

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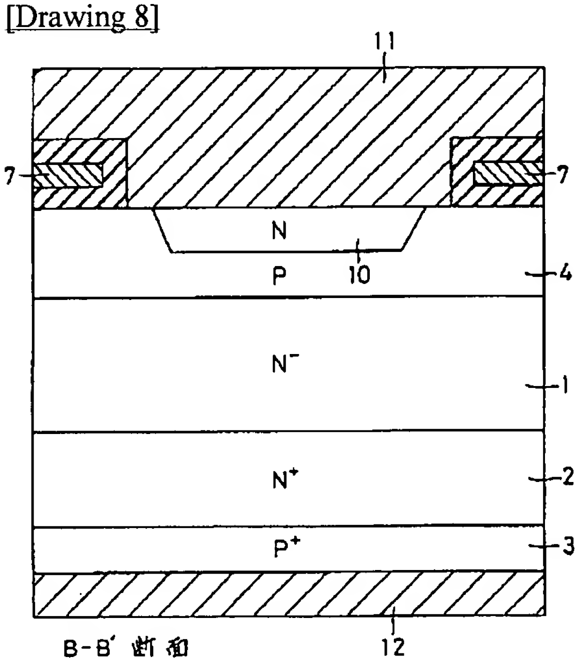

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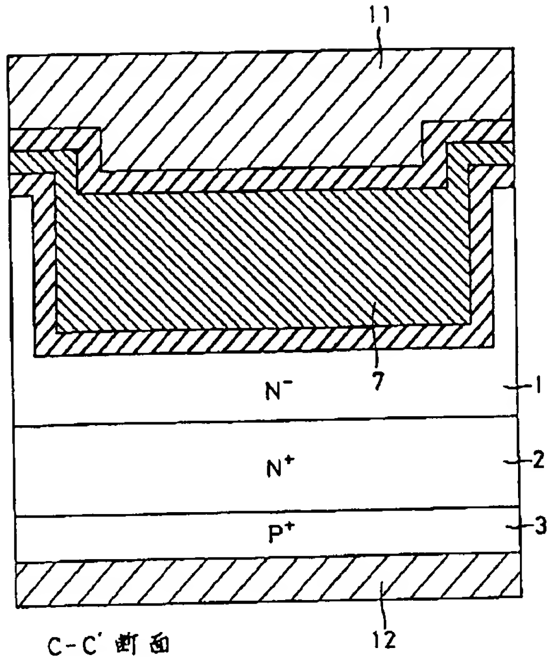

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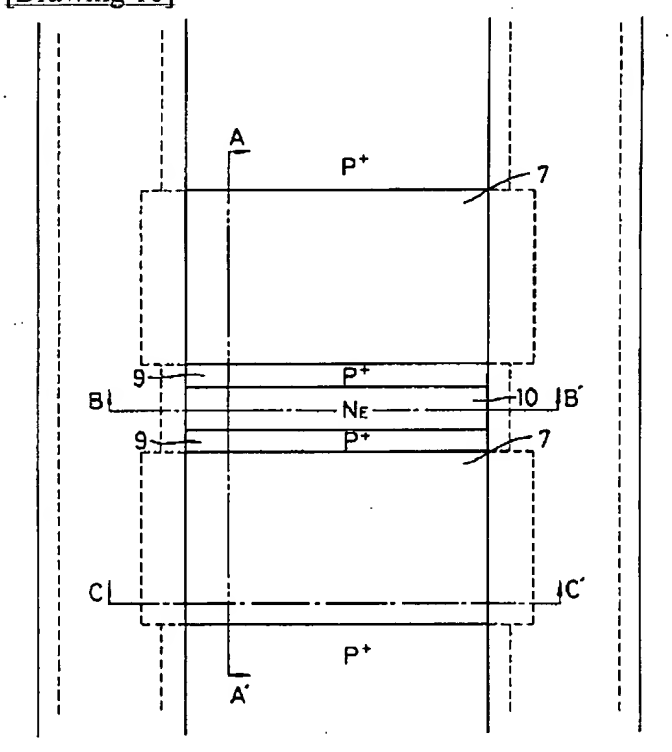

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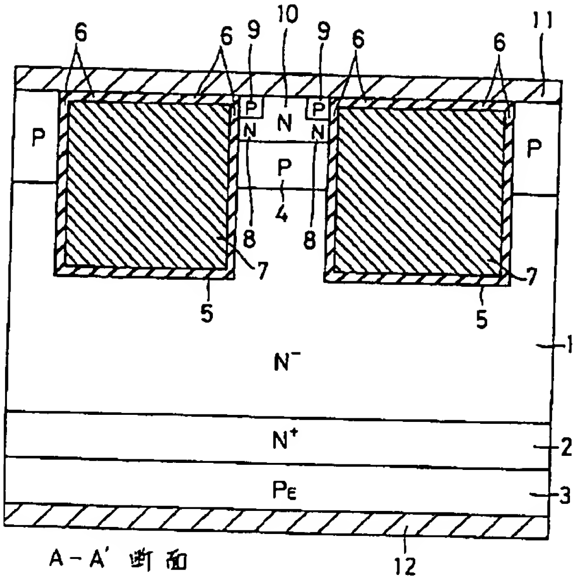

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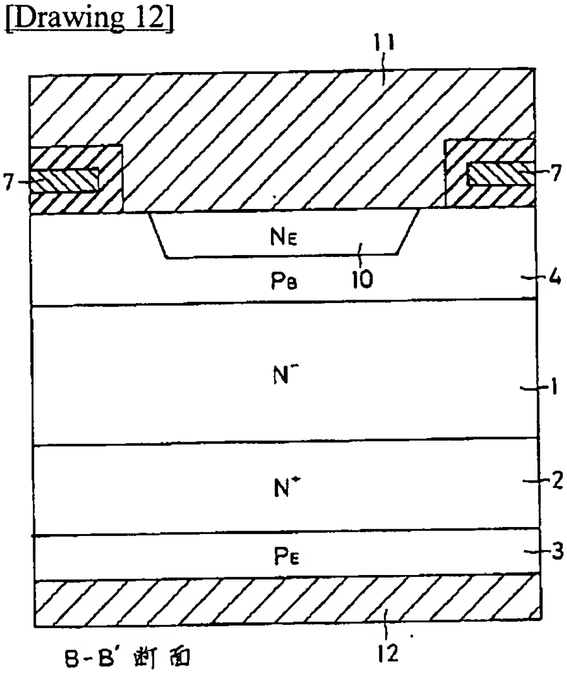

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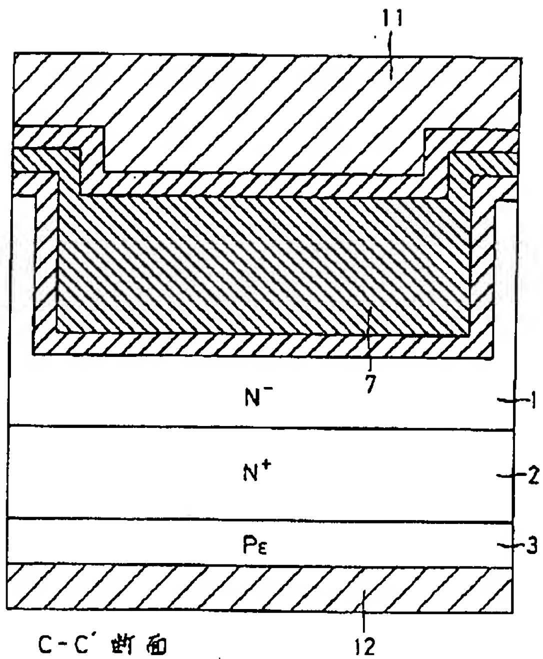

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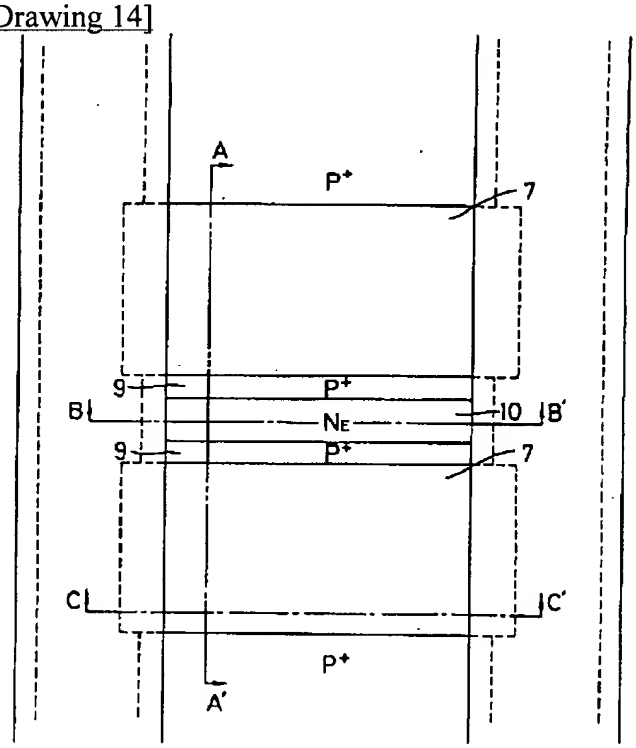

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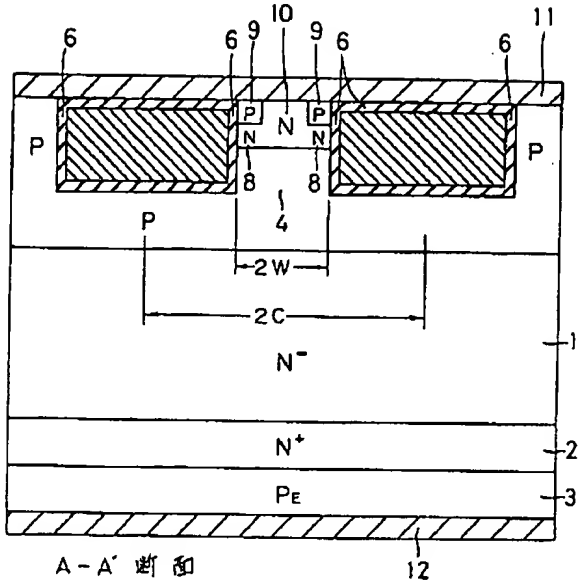

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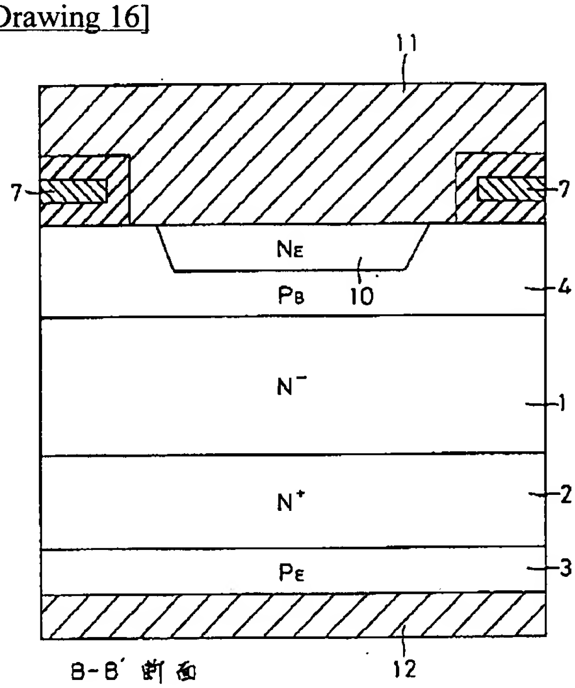

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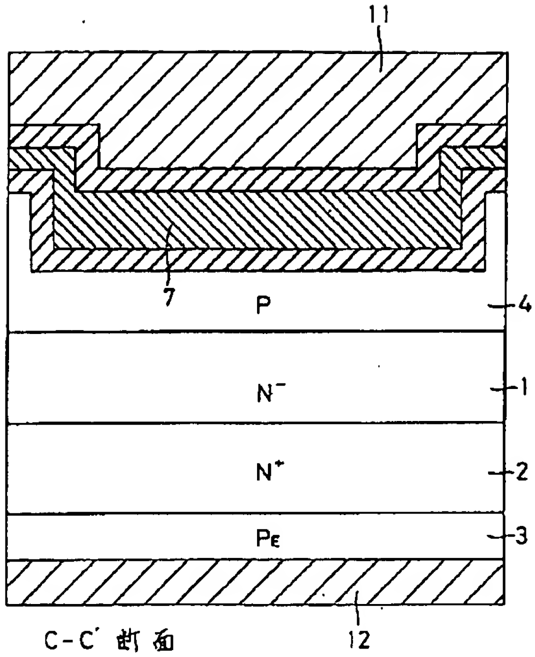

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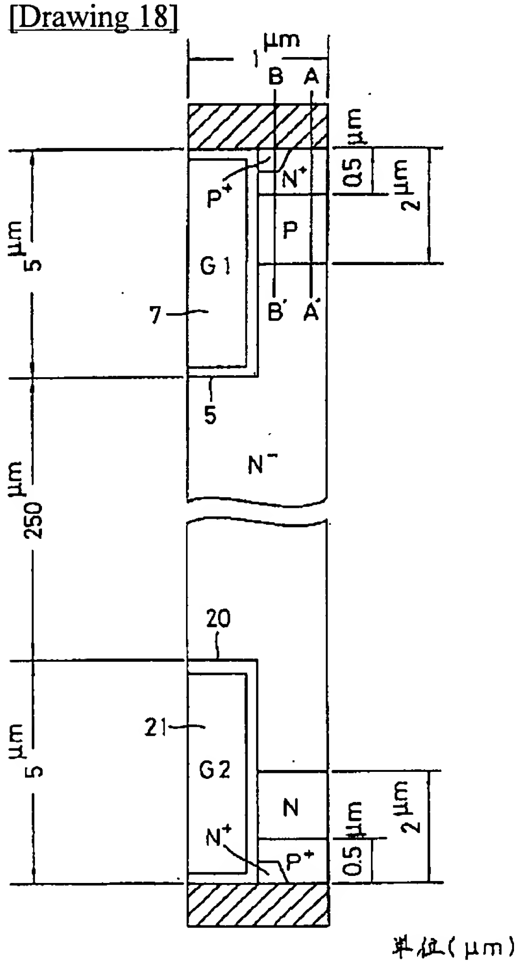

[Drawing 19]

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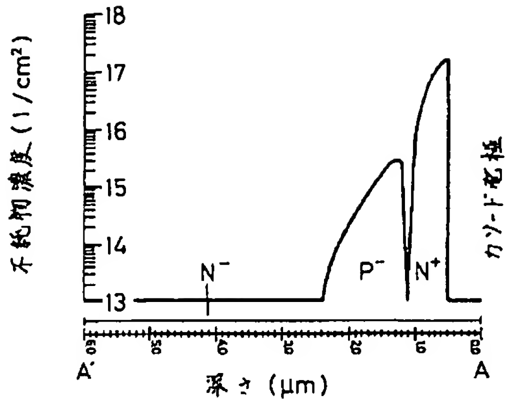
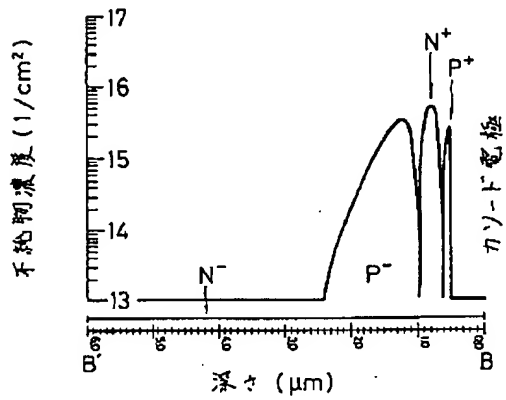


(b)



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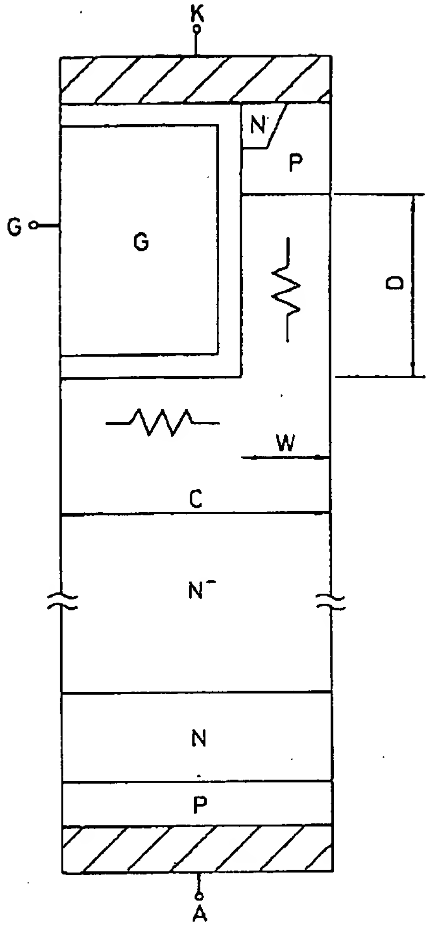

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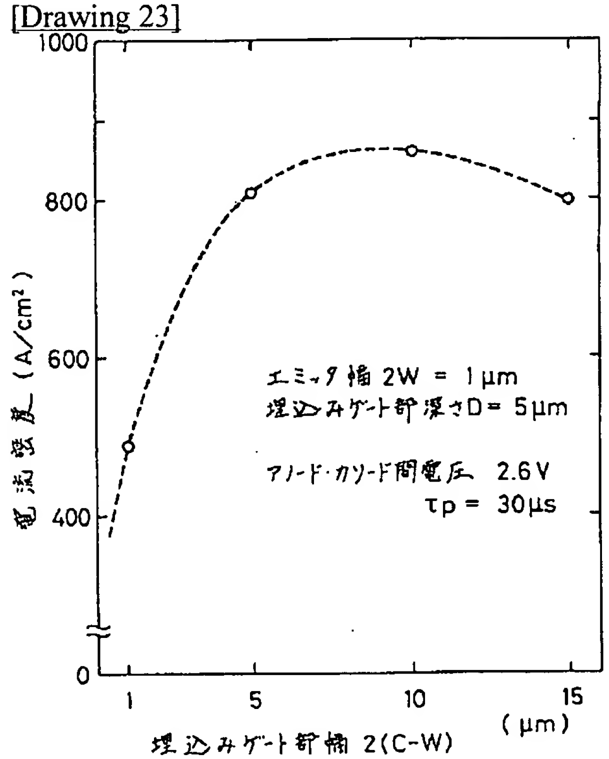

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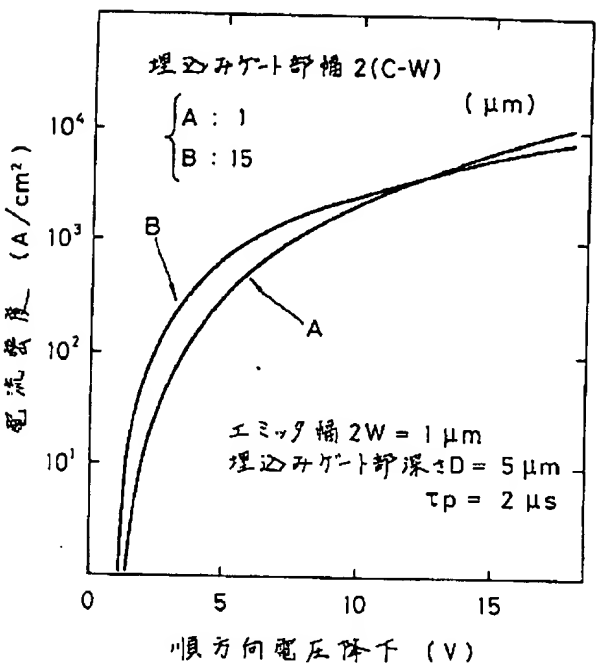

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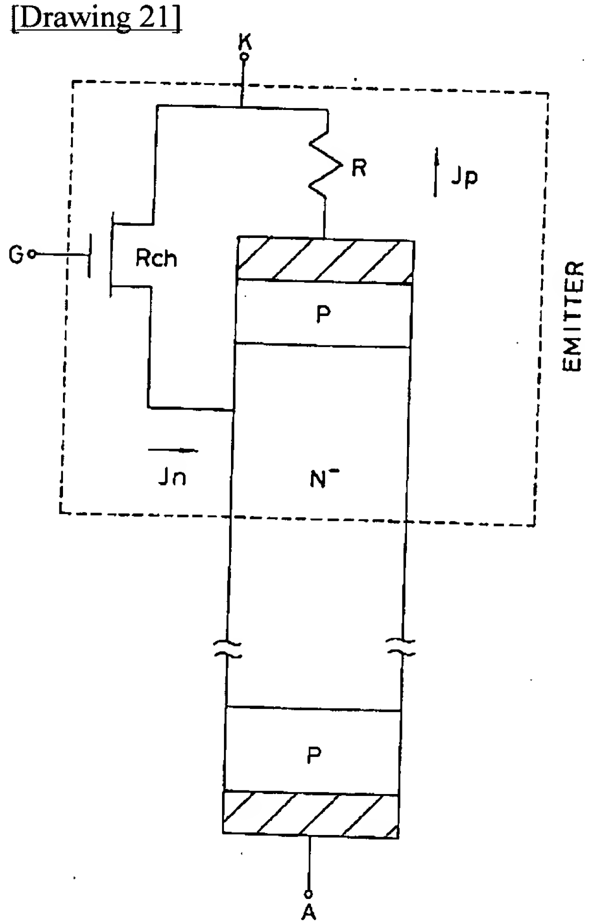

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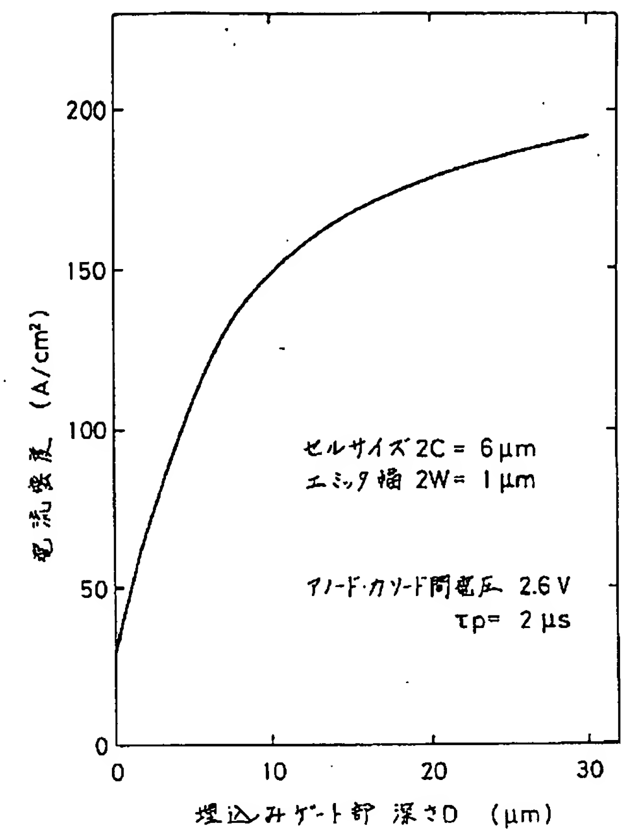

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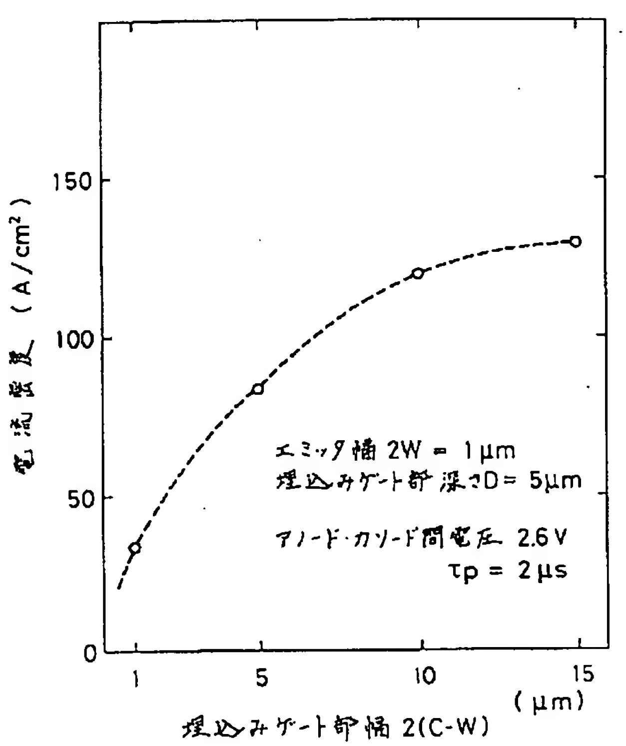

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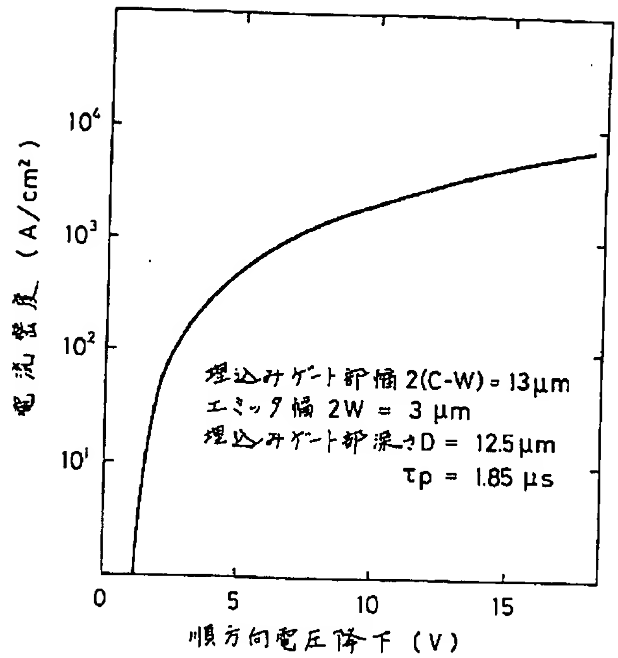

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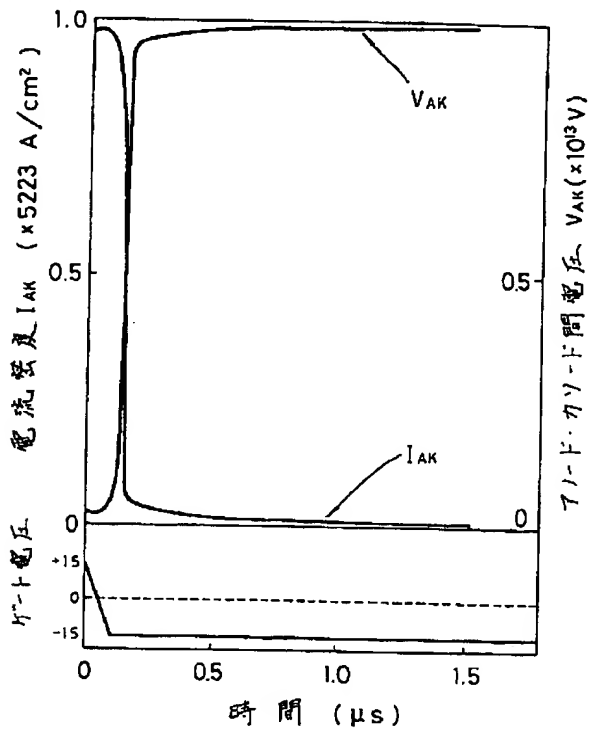

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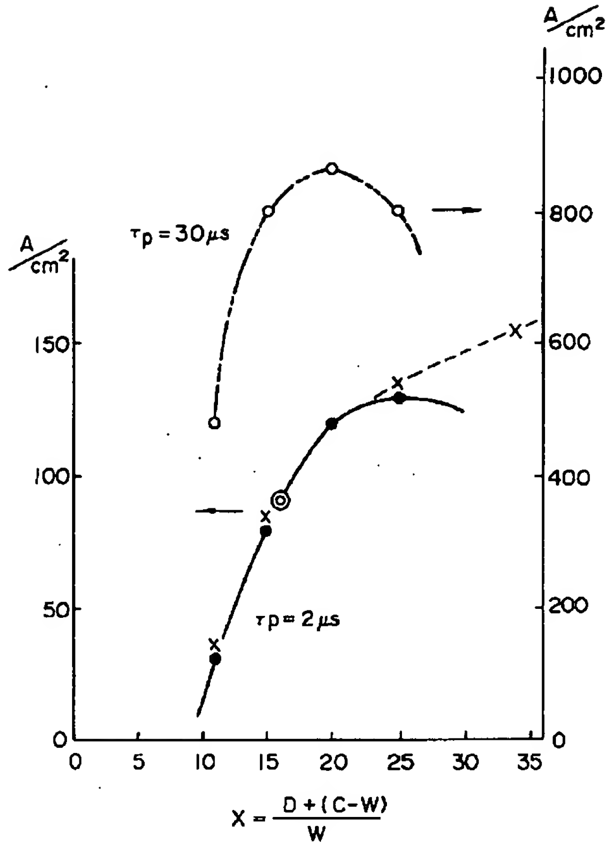

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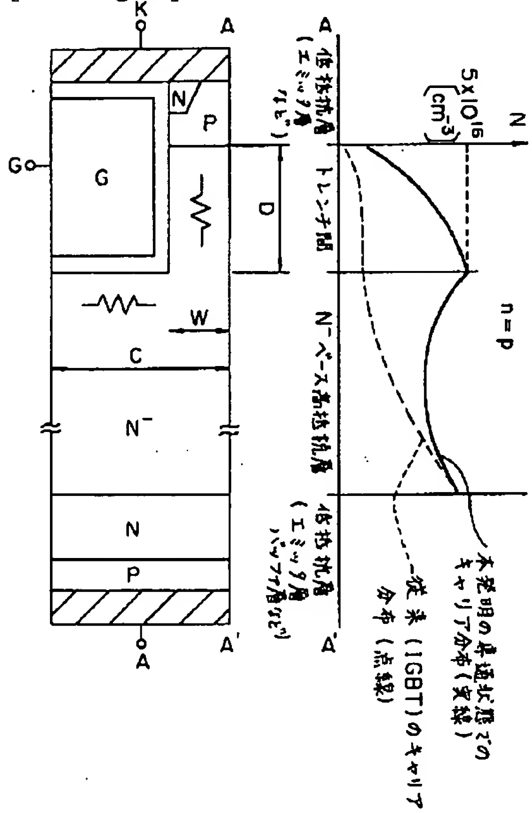

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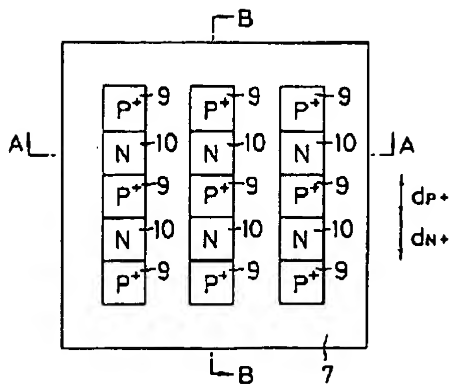

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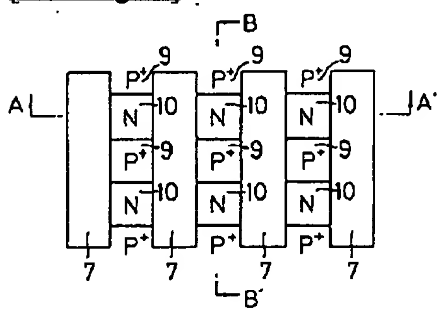

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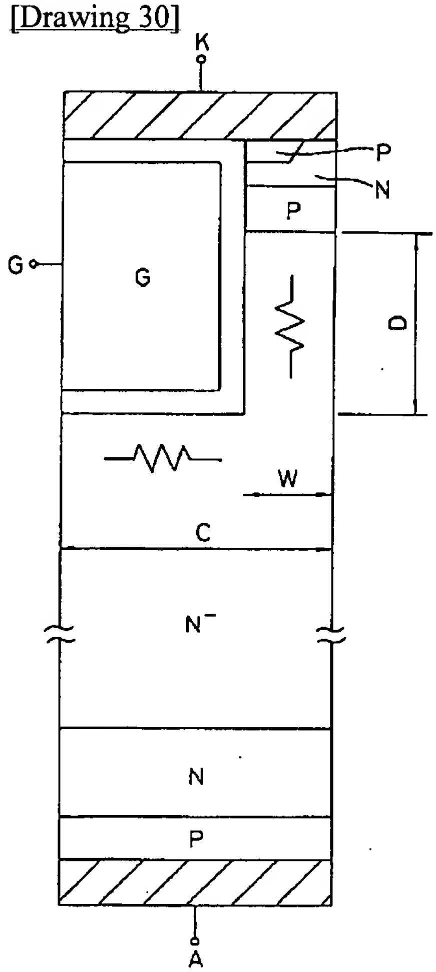

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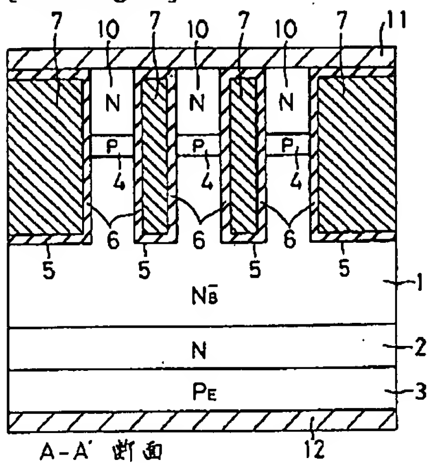

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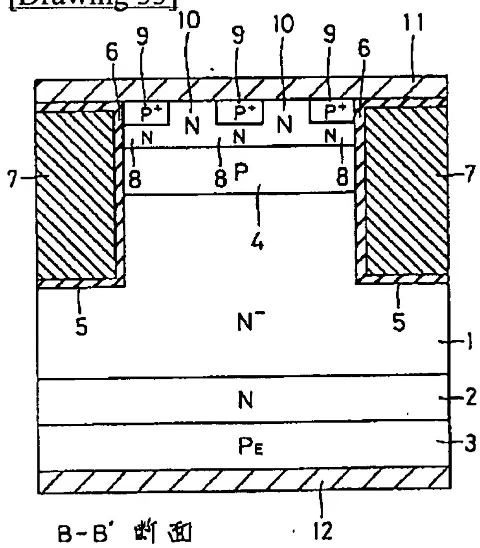

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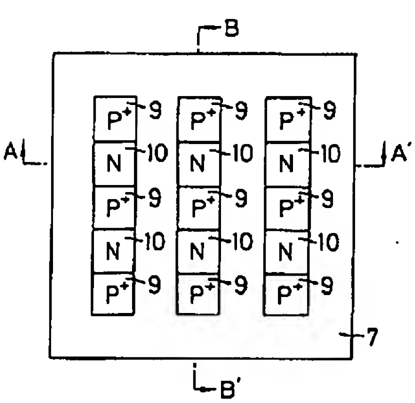

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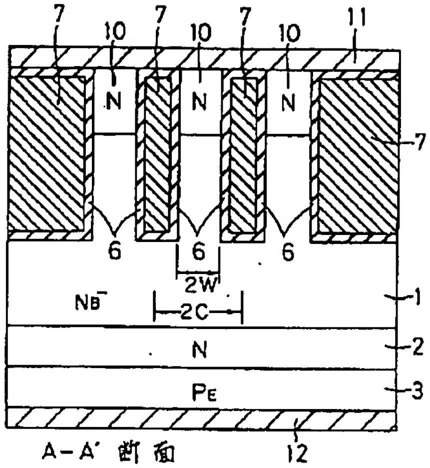

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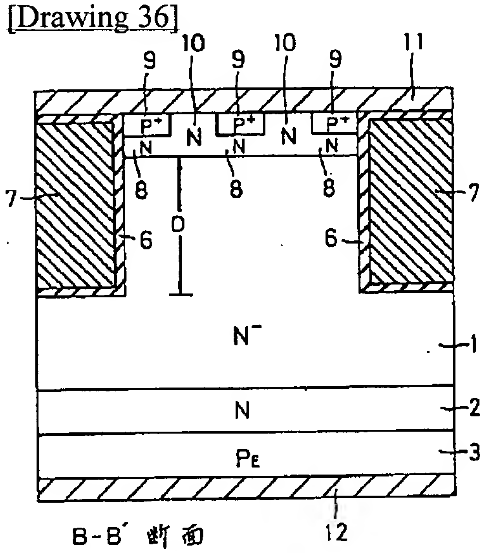

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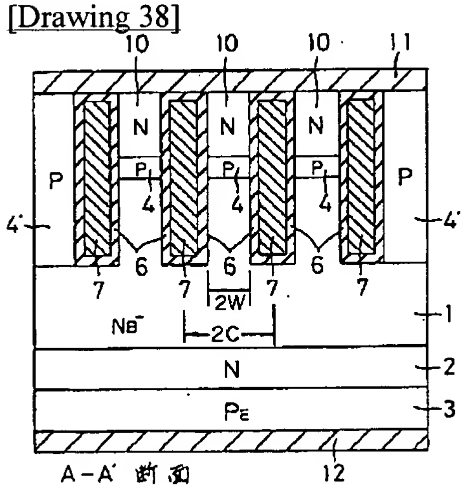

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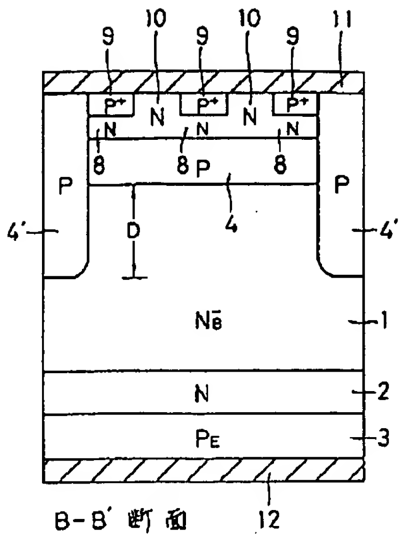
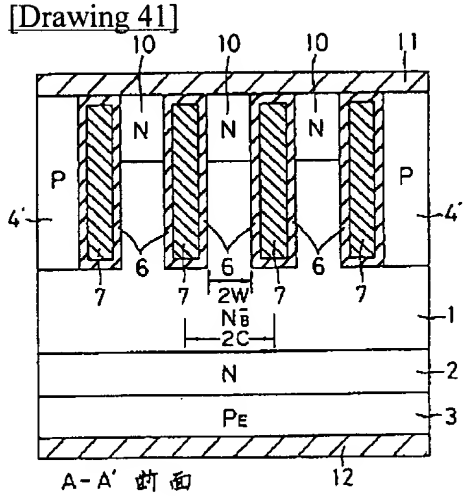


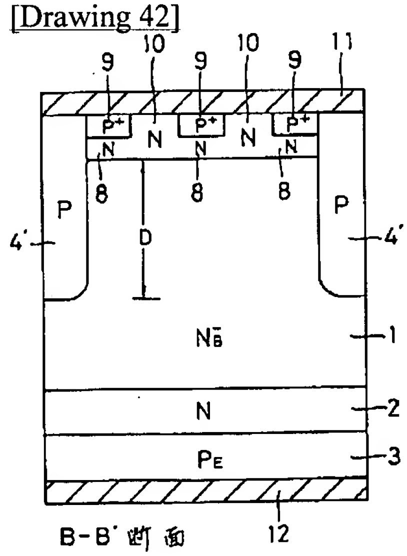
B-B' 断面

[Drawing 41]



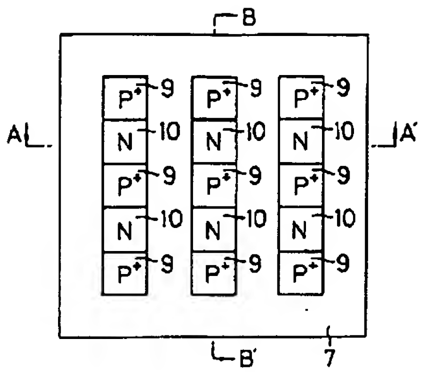
A-A' 断面

[Drawing 42]



B-B' 断面

[Drawing 43]



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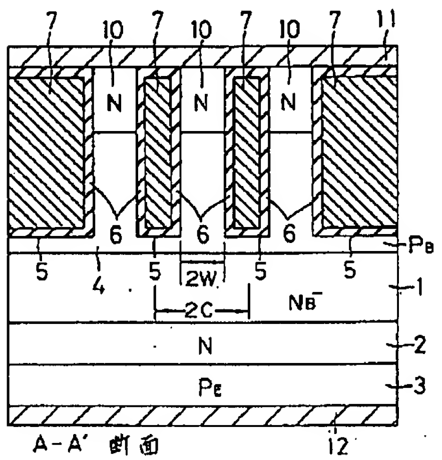

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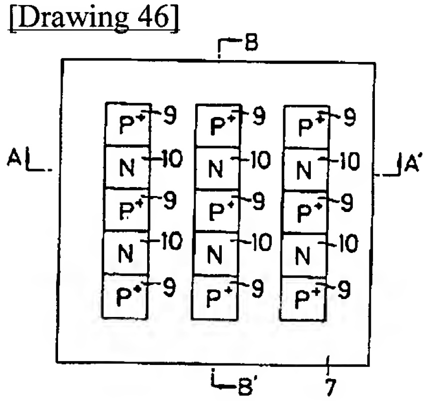

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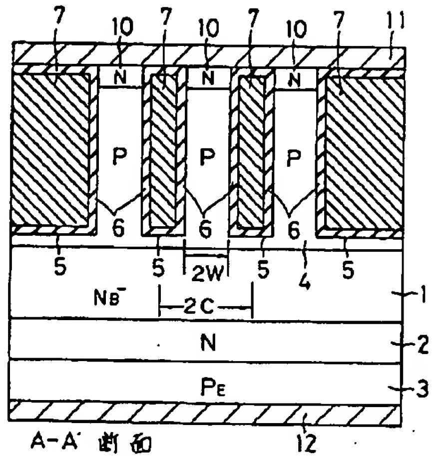

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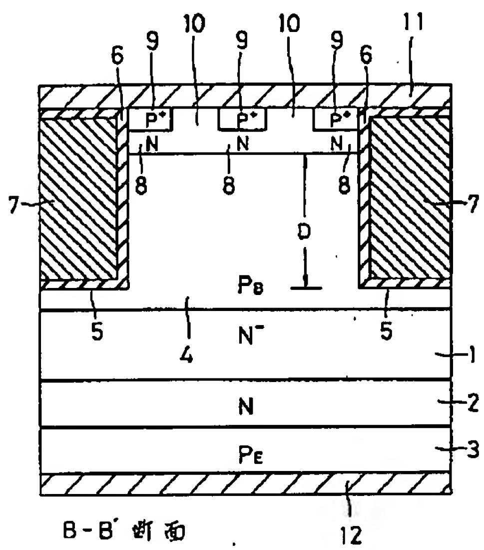

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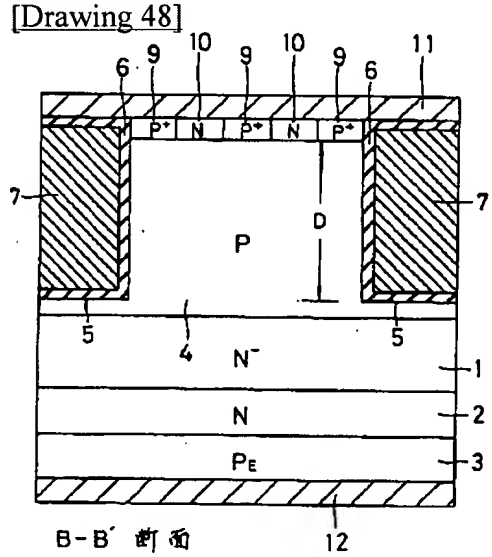

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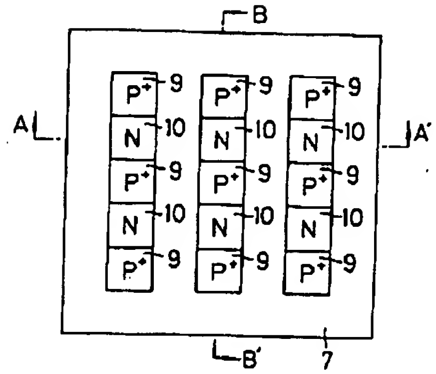

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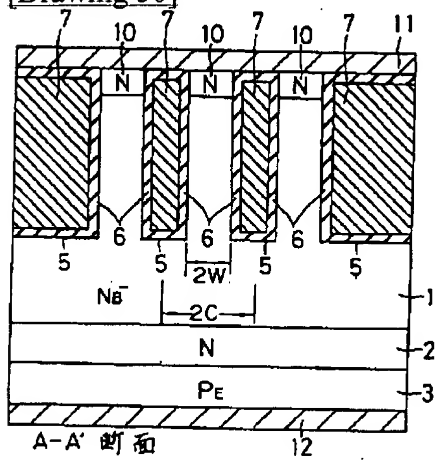

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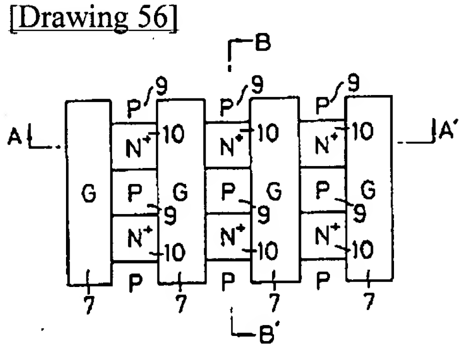
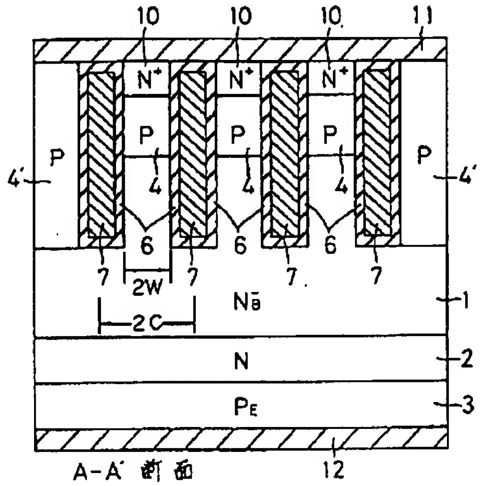
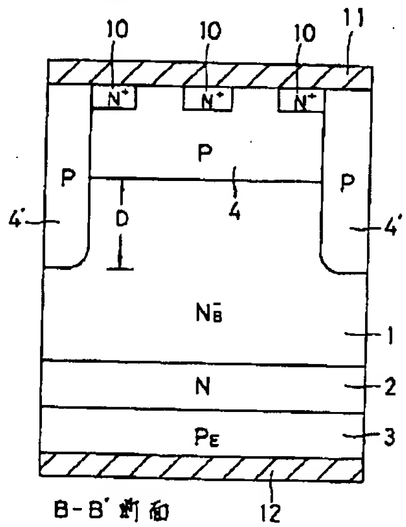


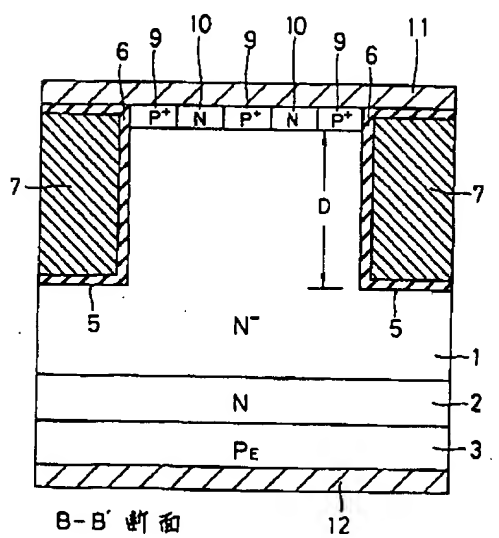
[Drawing 57]



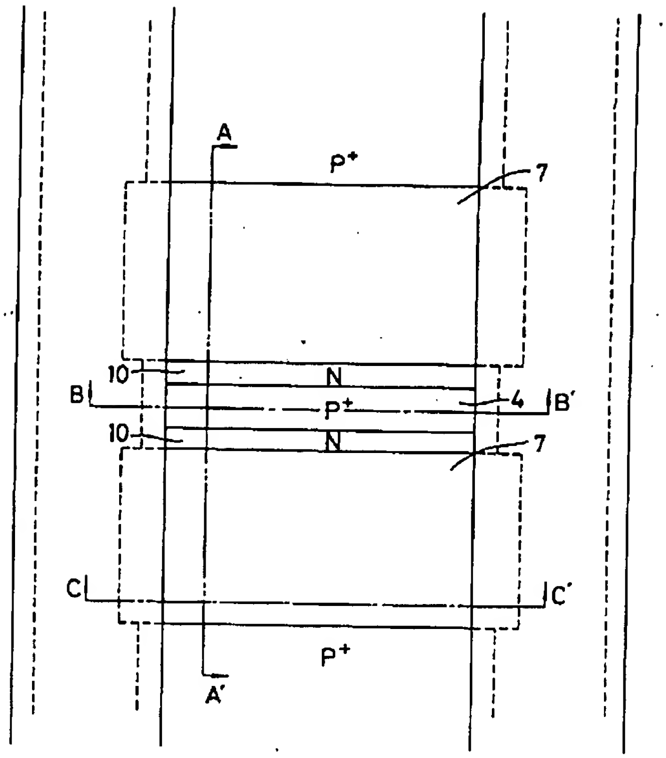
[Drawing 58]



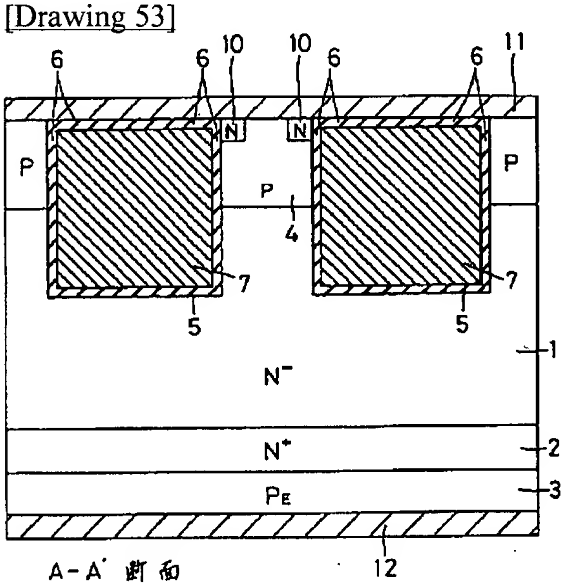
[Drawing 51]



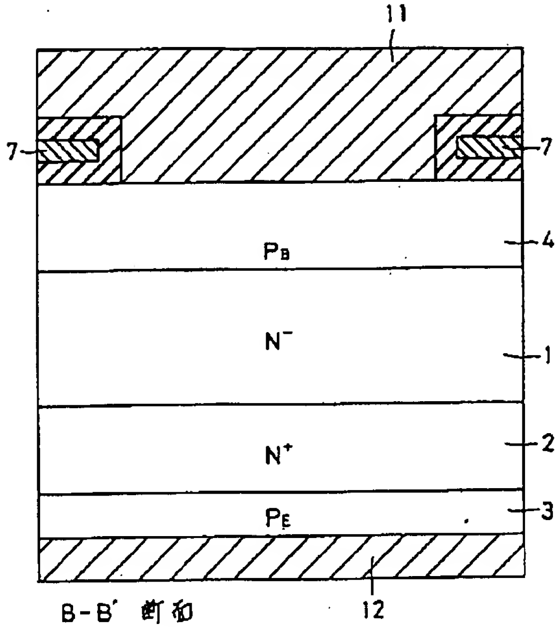
[Drawing 52]



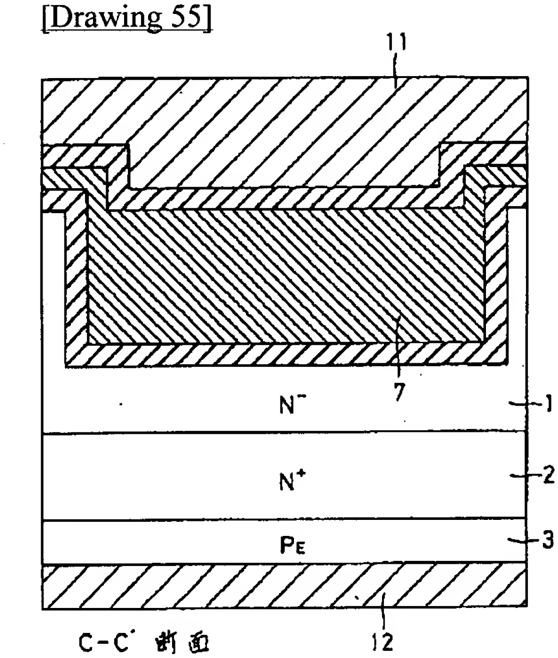
[Drawing 53]



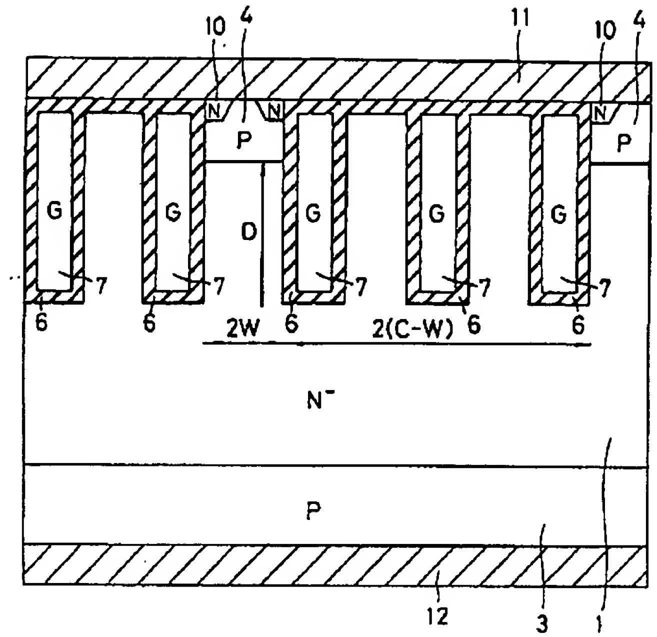
[Drawing 54]



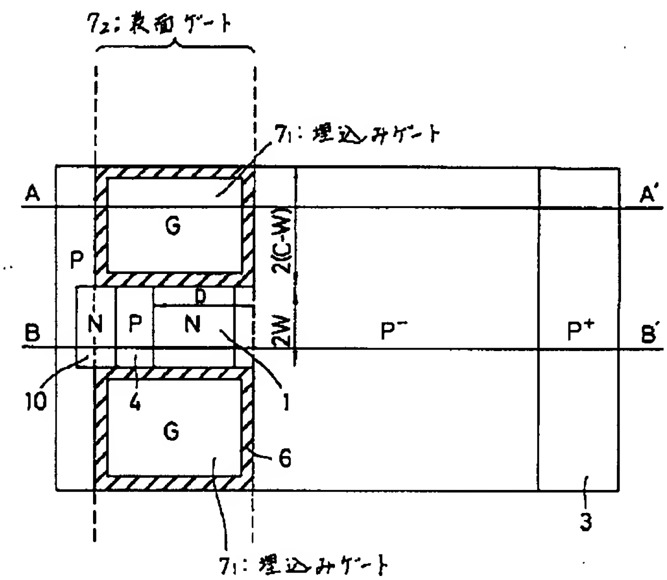
[Drawing 55]



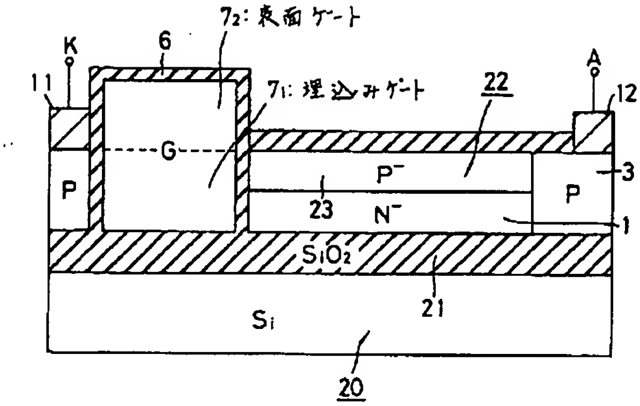
[Drawing 59]



[Drawing 60]



[Drawing 61]

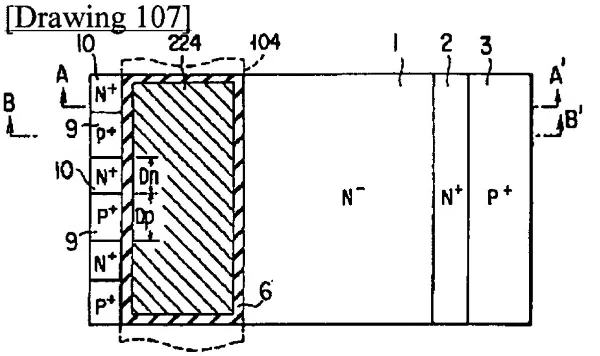


A- A' 断面

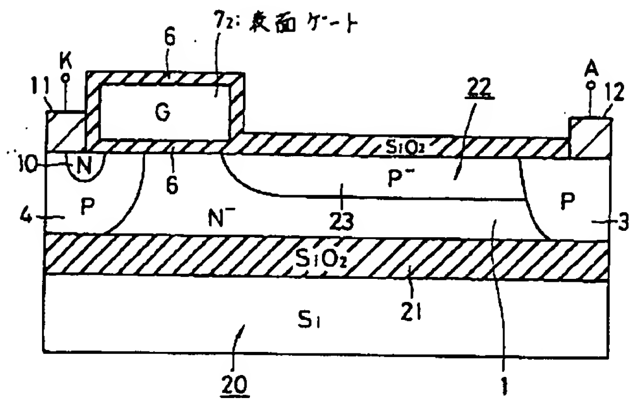
[Drawing 72]

ID=000074

[Drawing 107]

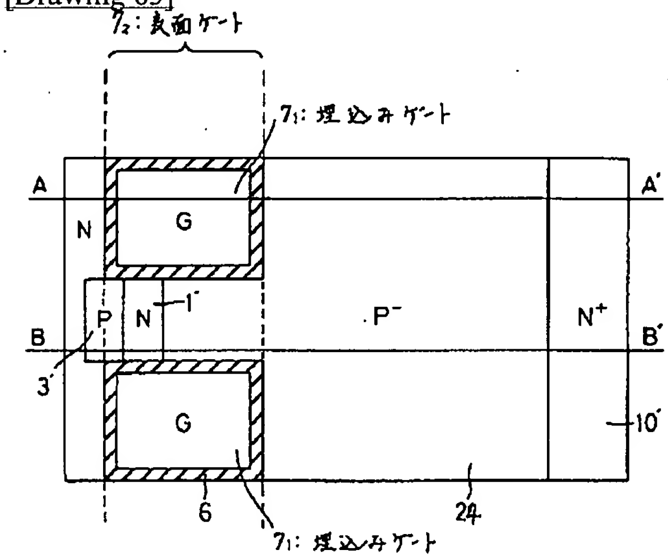


[Drawing 62]

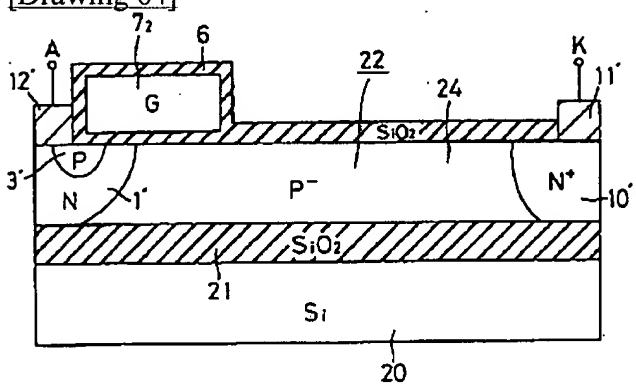


B-B' 断面

[Drawing 63]

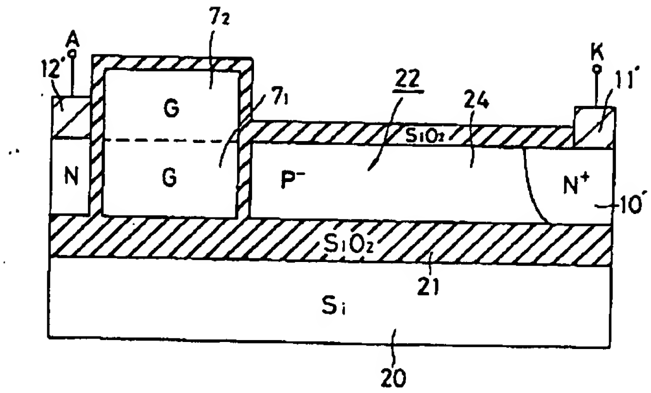


[Drawing 64]



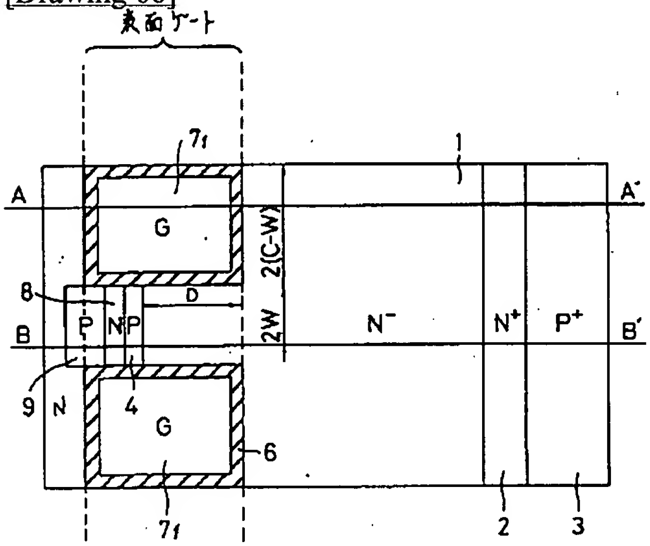
B-B' 断面

[Drawing 65]

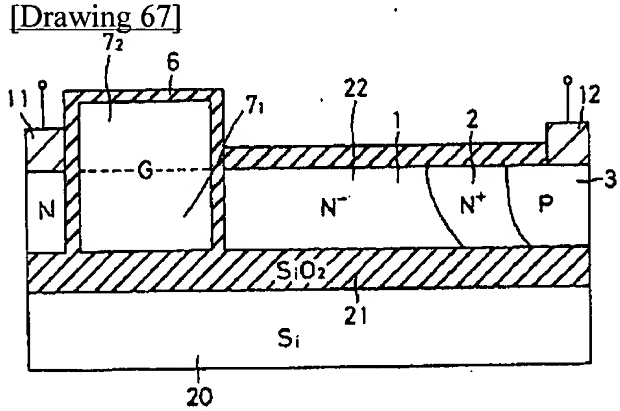


A-A' 断面

[Drawing 66]

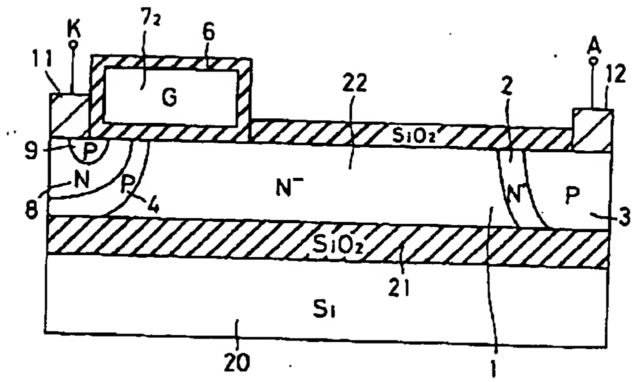


[Drawing 67]



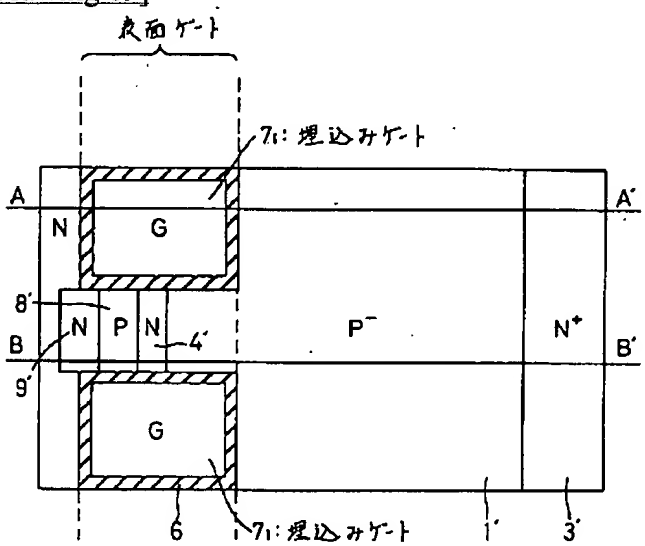
A-A' 断面

[Drawing 68]

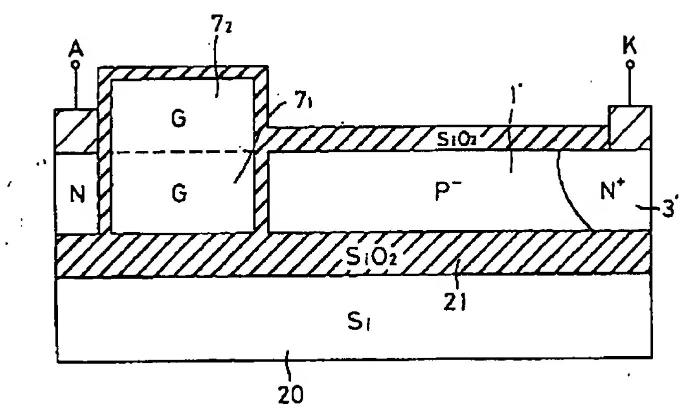


B-B' 断面

[Drawing 69]

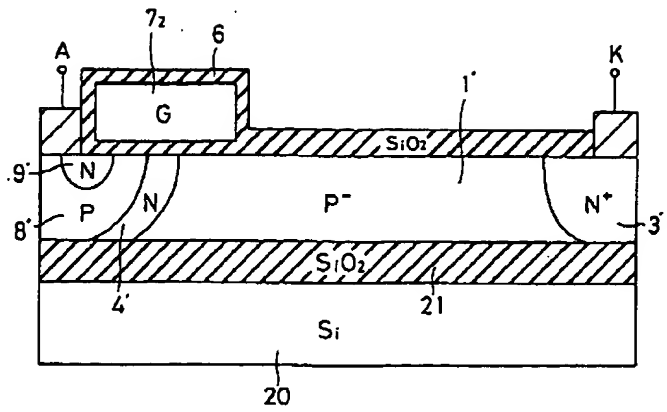


[Drawing 70]

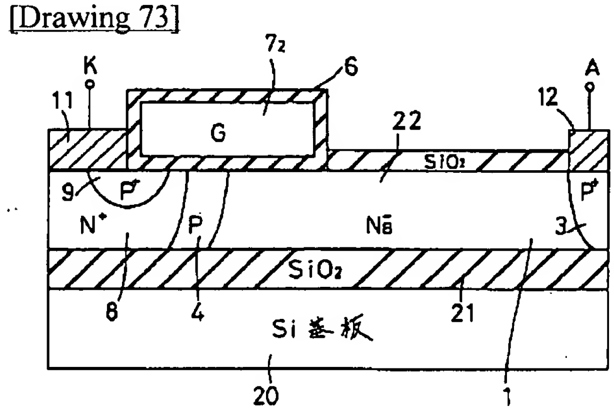


A-A' 断面

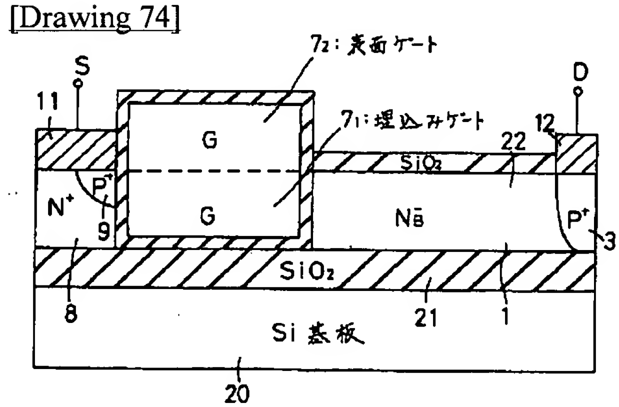
[Drawing 71]



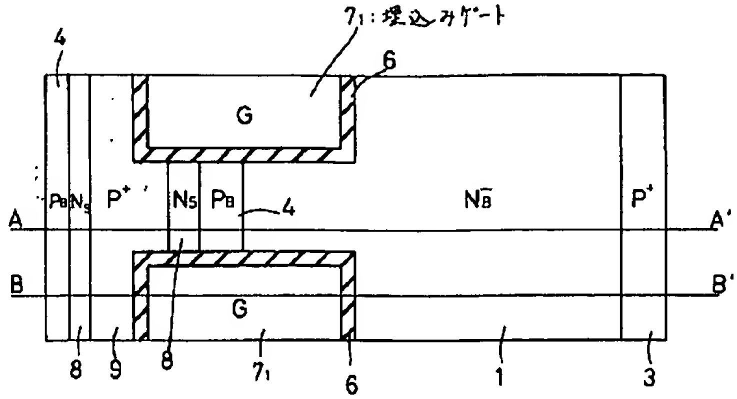
[Drawing 73]



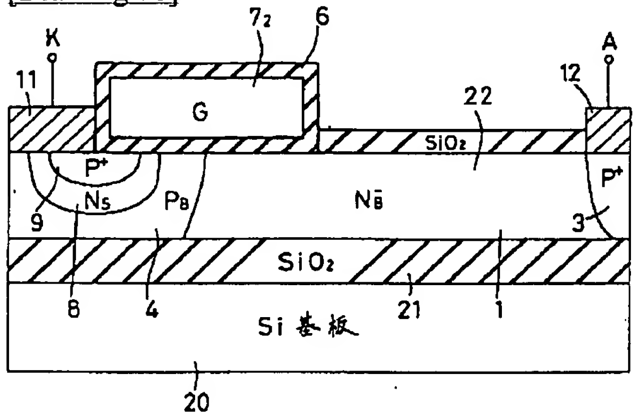
[Drawing 74]



[Drawing 75]

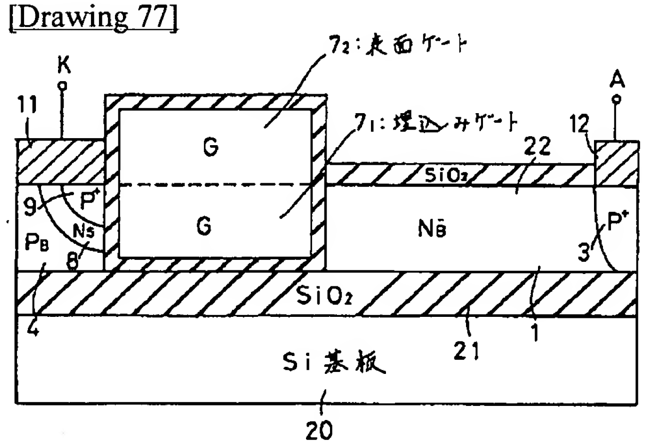


[Drawing 76]



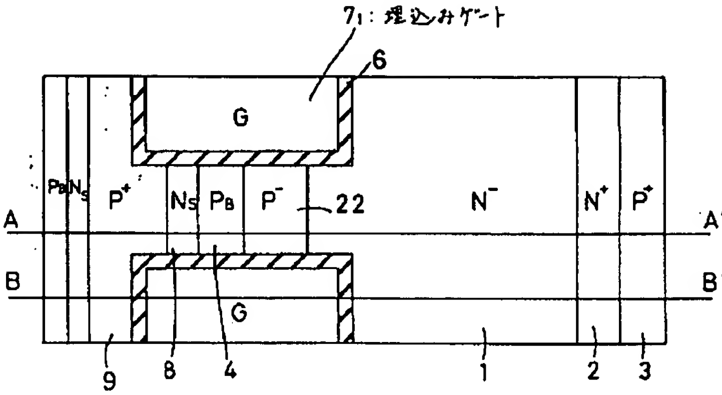
A－A' 断面

[Drawing 77]

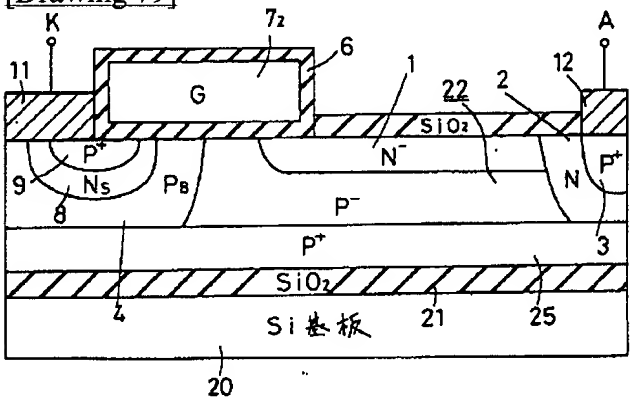


B－B' 断面

[Drawing 78]

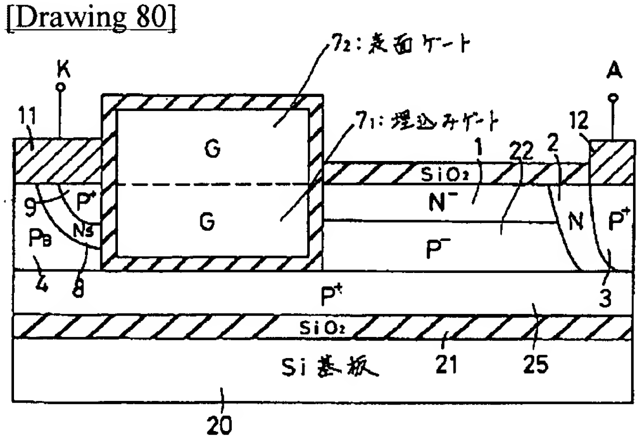


[Drawing 79]



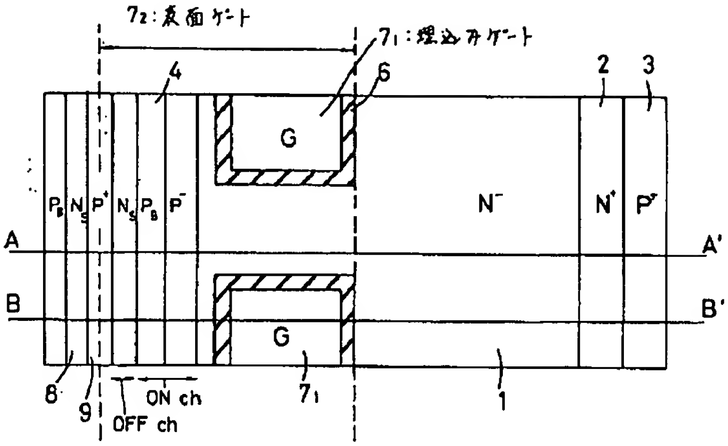
A−A′ 断面

[Drawing 80]

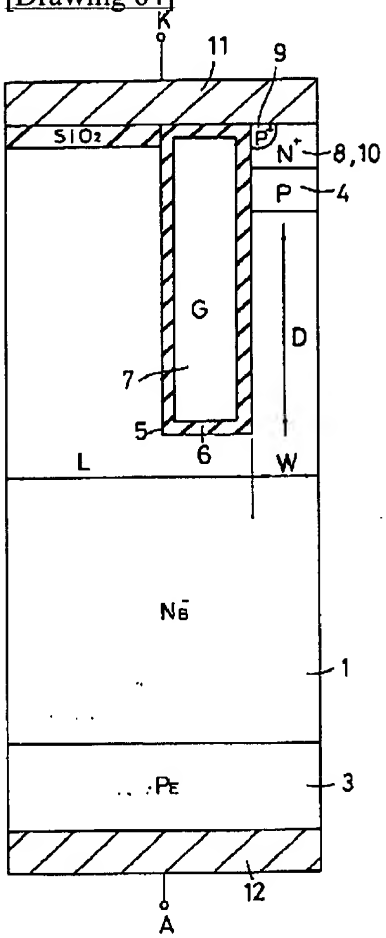


B−B′ 断面

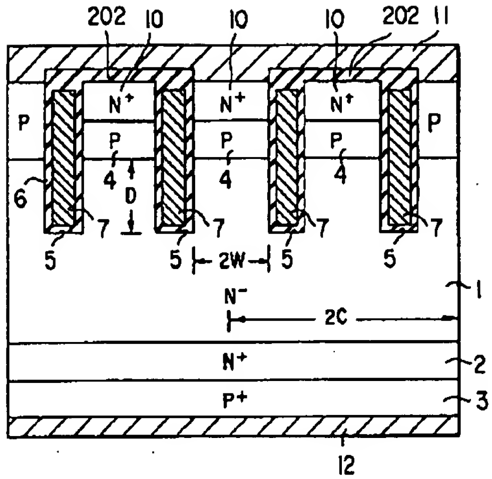
[Drawing 81]



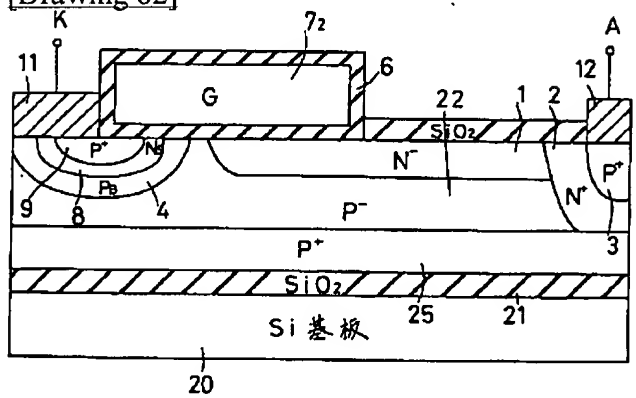
[Drawing 84]



[Drawing 97]

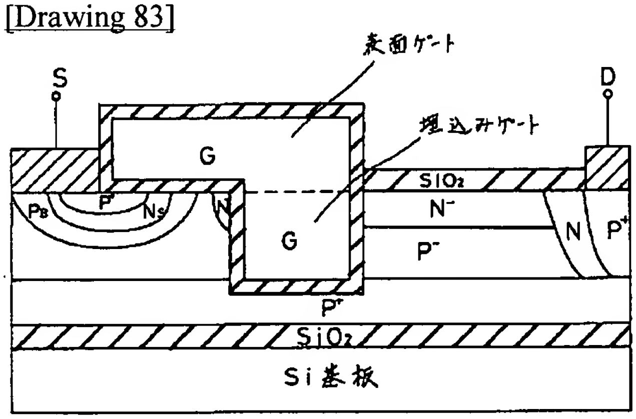


[Drawing 82]



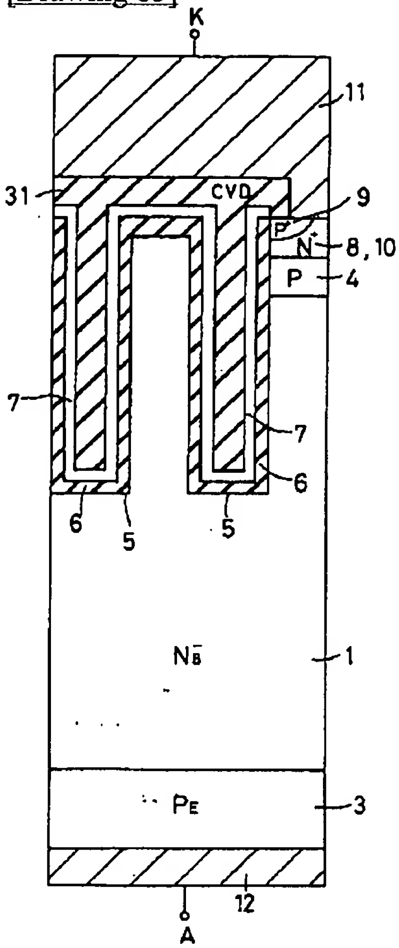
A－A' 断面

[Drawing 83]

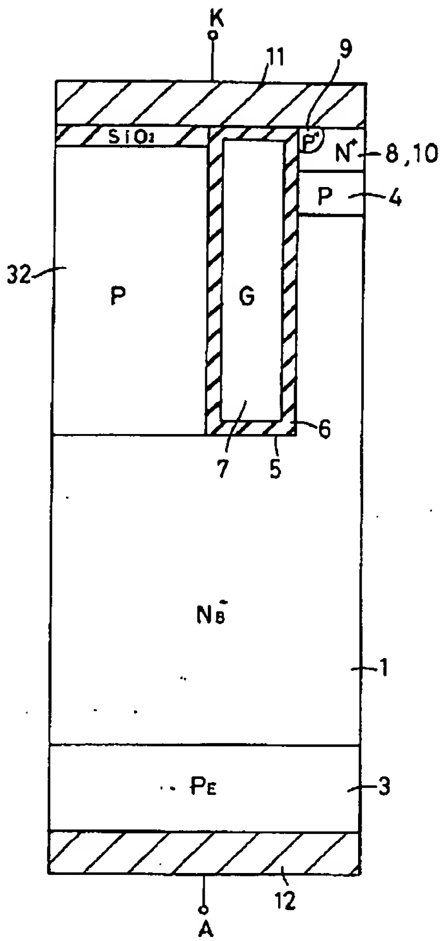


B－B' 断面

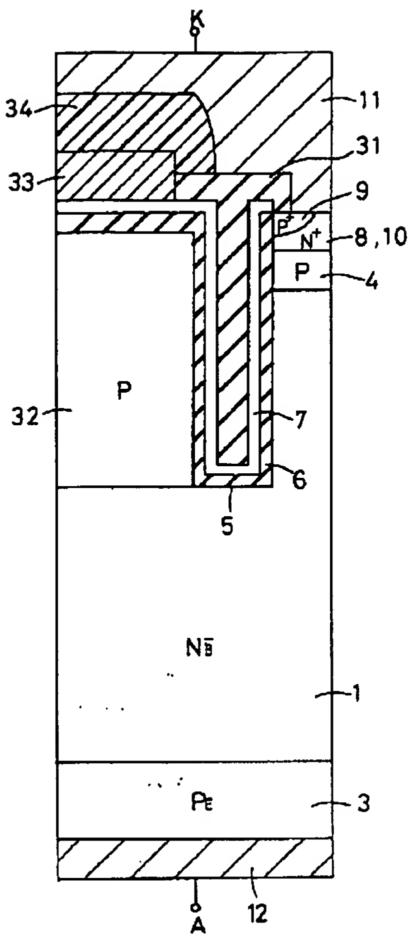
[Drawing 85]



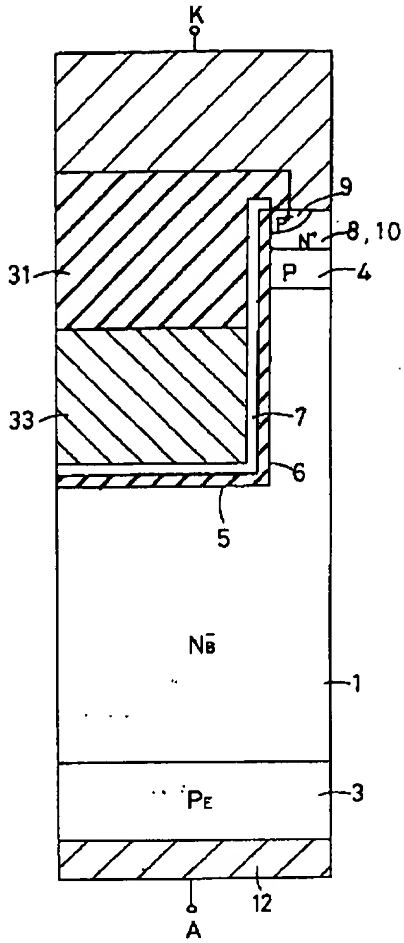
[Drawing 86]



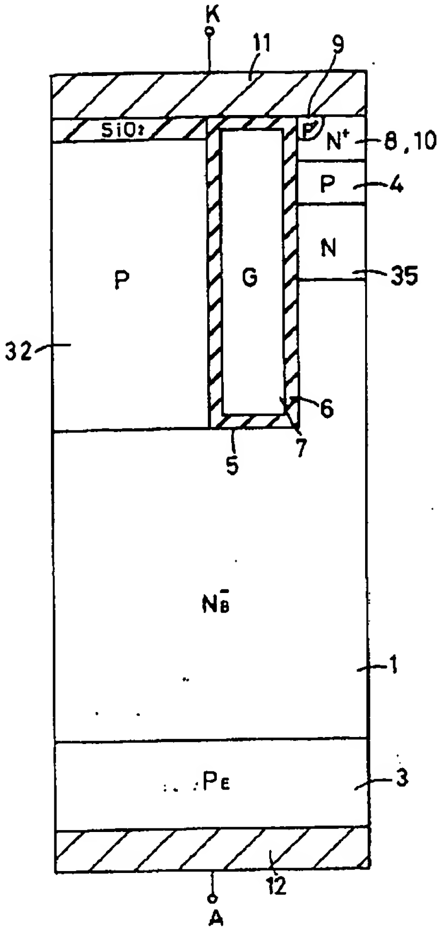
[Drawing 87]



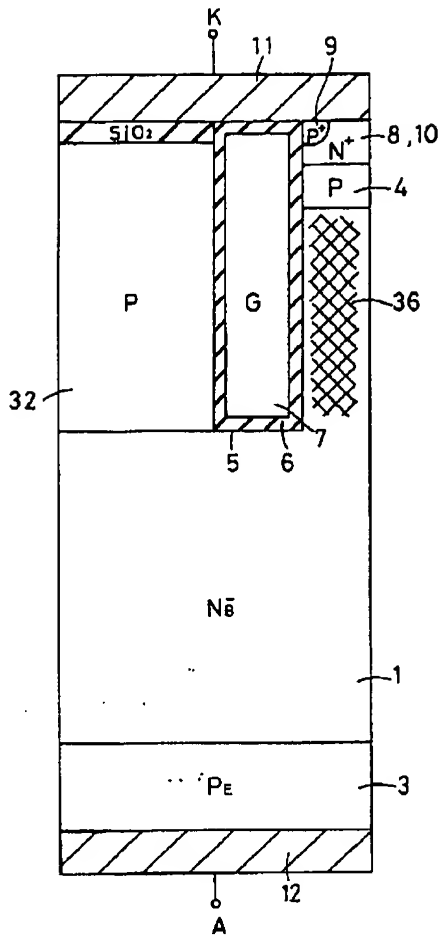
[Drawing 88]



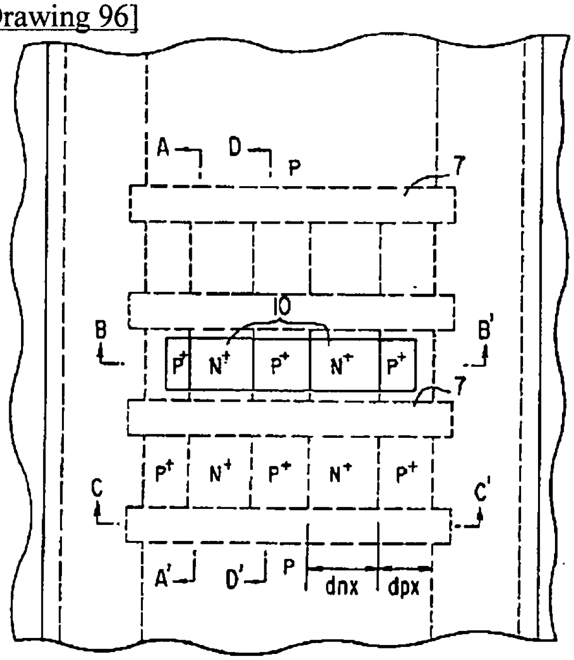
[Drawing 89]



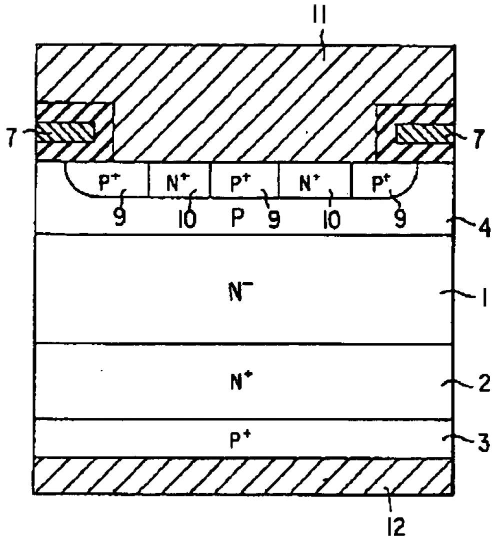
[Drawing 90]



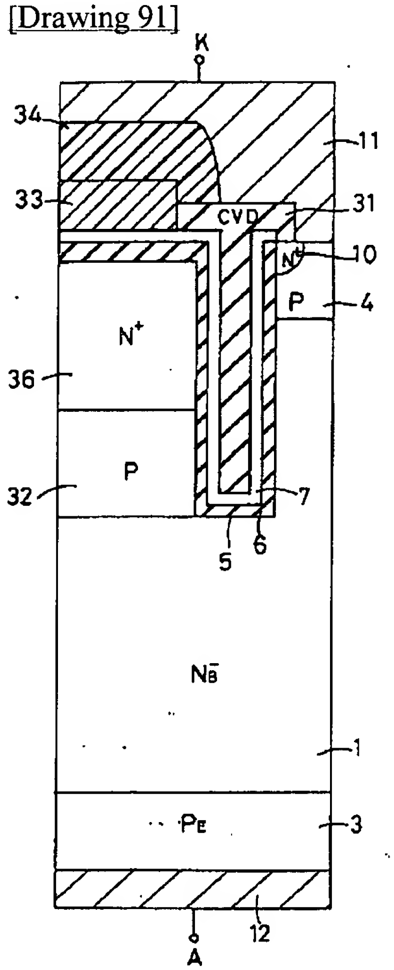
[Drawing 96]



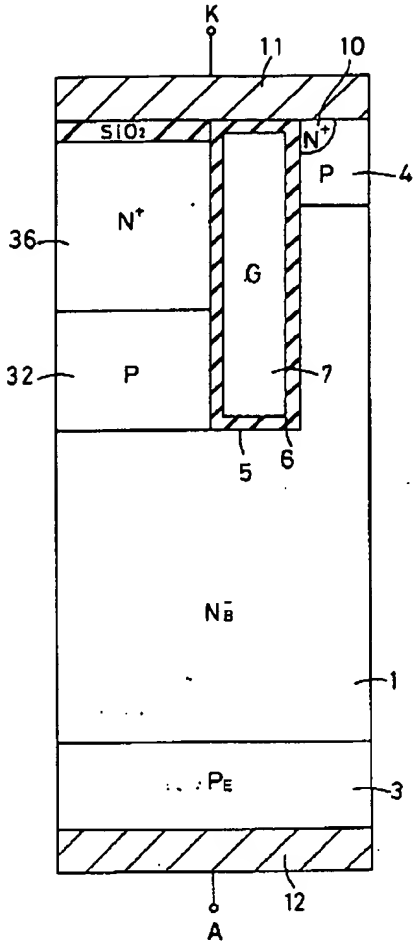
[Drawing 98]



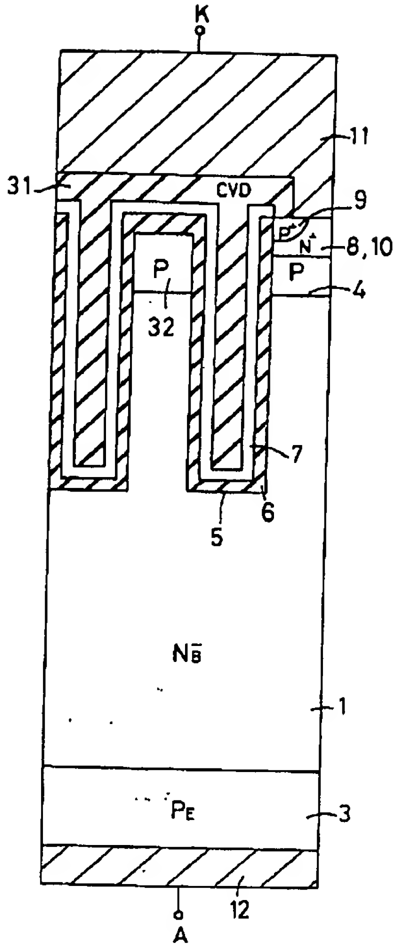
[Drawing 91]



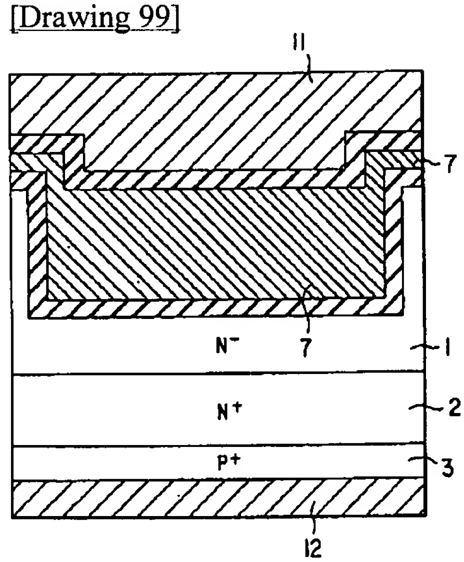
[Drawing 92]



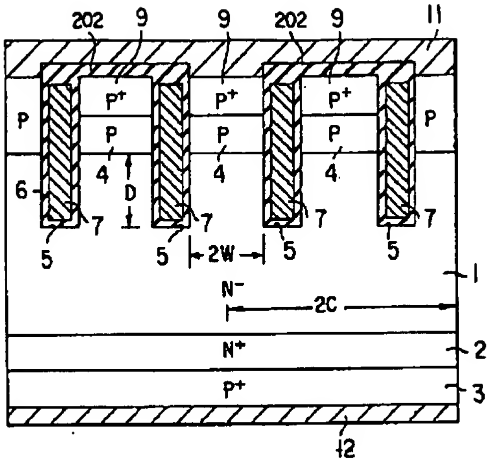
[Drawing 93]



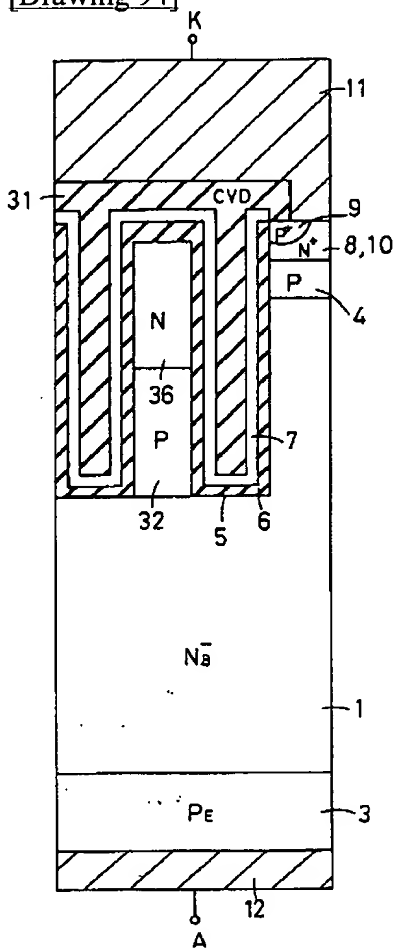
[Drawing 99]



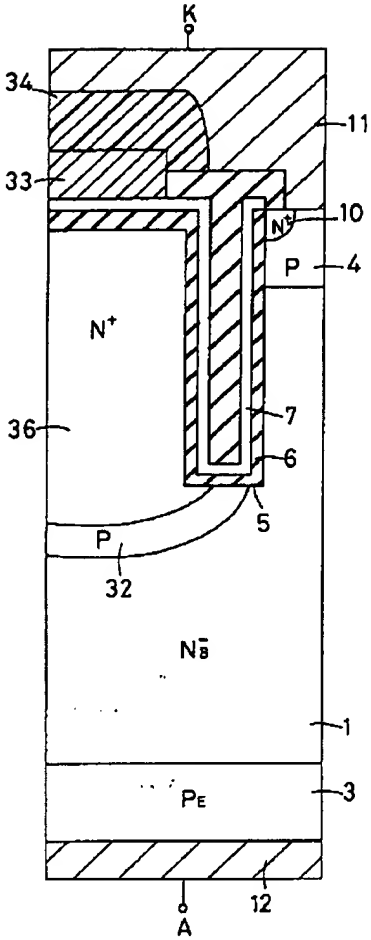
[Drawing 100]



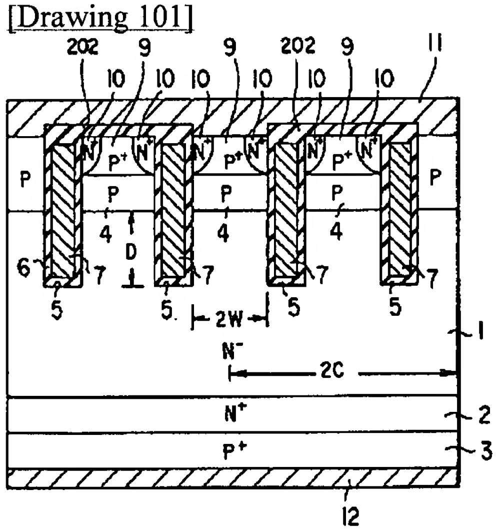
[Drawing 94]



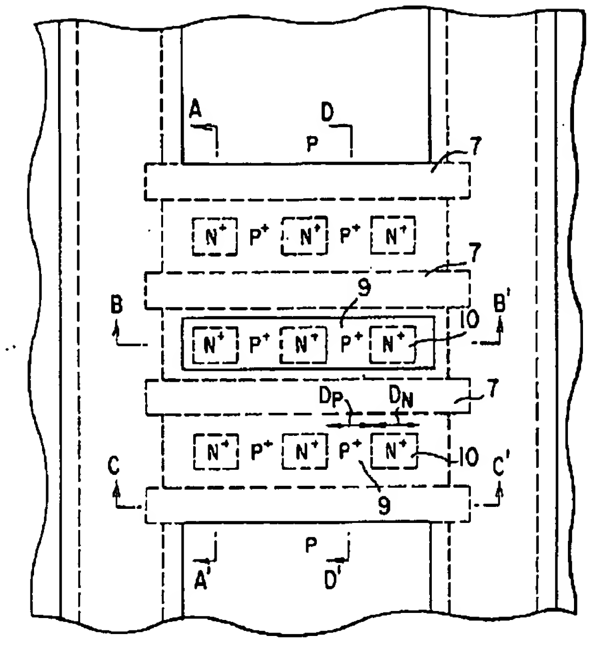
[Drawing 95]



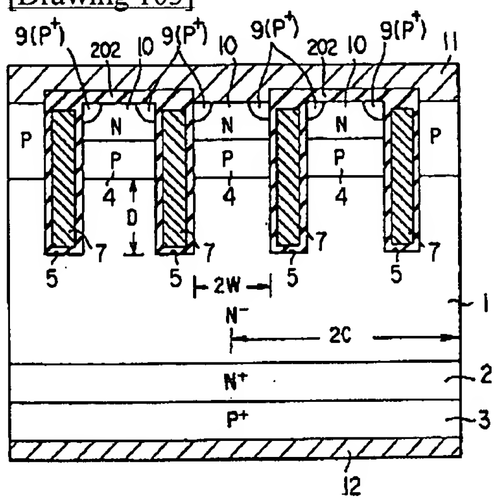
[Drawing 101]



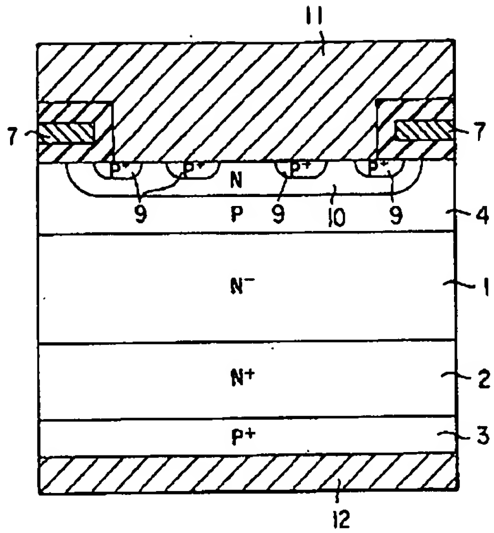
[Drawing 102]



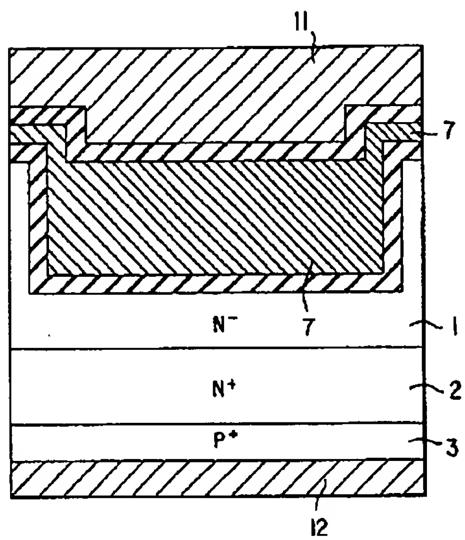
[Drawing 103]



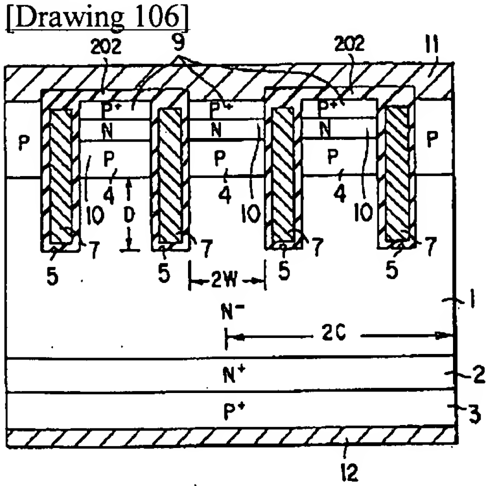
[Drawing 104]



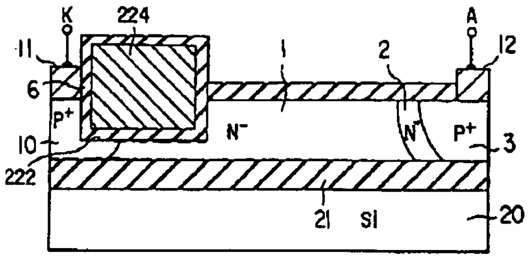
[Drawing 105]



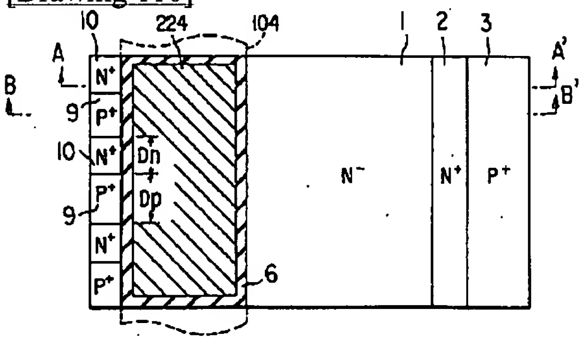
[Drawing 106]



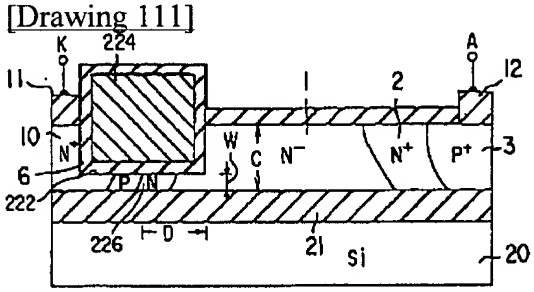
[Drawing 109]



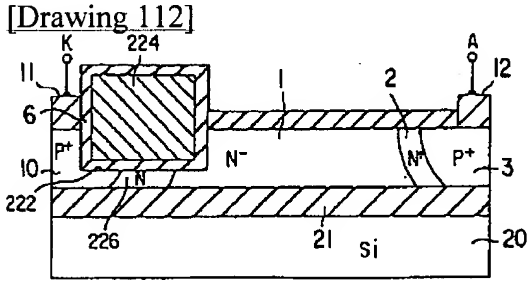
[Drawing 110]



[Drawing 111]



[Drawing 112]



[Translation done.]